Session 9: Panel — Testing Technology for Year 2000 Processor VLSIs

Organizer: K. Kinoshita, Osaka University Japan
Moderator: T. Yamada , Meiji University, Japan
Panelists:
T. Gheewala - CrossCheck, USA
K. Hatayama - Hitachi, Japan
F. Hirose - Fujitsu, Japan
M. Takada - NEC, Japan

Session 10: Panel — Effectiveness of BIST in Consumer Products

Organizer: Y. Zorian, AT&T Bell Laboratories, USA
Moderator: V.K. Agarwal, McGill University, Canada
Panelists: [to be announced]

Session 11: Design for Testability

Chair: M.W.T. Wong, Hong Kong Polytechnic

Session 12: IDDQ and Bridging Faults

Chair: Y-S. Tao, Information Technology Institute, Singapore

Session 13: Testability Analysis

Chair: H. Hiraishi, Kyoto Sangyo University, Japan

Session 14: Self-Checking

Chair: J-L. Chen, Beijing University of Post and Telecommunication, China