Asian Test Symposium Most-Cited Papers in 30 Years

Most-Cited Paper Awards

1. A SmartBIST variant with guaranteed encoding
   B. Koenemann, C. Barnhart, B. Keller, T. Snethen, O. Farnsworth, D. Wheater
   10th Asian Test Symposium, 2001
   DOI: 10.1109/ATS.2001.990304

2. On-chip TSV testing for 3D IC before bonding using sense amplification
   P.-Y. Chen, C.-W. Wu, D.-M. Kwai
   18th Asian Test Symposium, 2009
   DOI: 10.1109/ATS.2009.42

3. Timing-aware ATPG for high quality at-speed testing of small delay defects
   X. Lin, K.-H. Tsai, C. Wang, M. Kassab, J. Rajski, T. Kobayashi, R. Klingenberg, Y. Sato, S. Hamada, T. Aikyo
   15th Asian Test Symposium, 2006
   DOI: 10.1109/ATS.2006.261012

Most-Cited Papers

4. Resource allocation and test scheduling for concurrent test of core-based SOC design
   Y. Huang, W.-T. Cheng, C.-C. Tsai, N. Mukherjee, O. Samman, Y. Zaidan, S.M. Reddy
   10th Asian Test Symposium, 2001
   DOI: 10.1109/ATS.2001.990293

5. A gated clock scheme for low power scan testing of logic ICs or embedded cores
   Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch
   10th Asian Test Symposium, 2001
   DOI: 10.1109/ATS.2001.990291

6. A family of logical fault models for reversible circuits
   I. Polian, T. Fiehn, B. Becker, J.P. Hayes
   14th Asian Test Symposium, 2005
   DOI: 10.1109/ATS.2005.9

7. An experimental analysis of spot defects in SRAMs: Realistic fault models and tests
   S. Hamdioui, A.J. Van De Goor
   9th Asian Test Symposium, 2000
   DOI: 10.1109/ATS.2000.893615

8. Testing for missing-gate faults in reversible circuits
   J.P. Hayes, I. Polian, B. Becker
   13th Asian Test Symposium
   DOI: 10.1109/ATS.2004.84

9. New capabilities of OBIRCH method for fault localization and defect detection
   K. Nikawa, S. Inoue
   6th Asian Test Symposium, 1997
   DOI: 10.1109/ATS.1997.643961

10. Test methodology for interconnect structures of LUT-based FPGAs
    H. Michinishi, T. Yokohira, T. Okamoto, T. Inoue, H. Fujiwara
    5th Asian Test Symposium, 1996
    DOI: 10.1109/ATS.1996.555139

10. Peak-power reduction for multiple-scan circuits during test application
    K.-J. Lee, T.-C. Huang, J.-J. Chen
    9th Asian Test Symposium, 2000
    DOI: 10.1109/ATS.2000.893666

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