ATS 2014 Advance Program

Nov. 16

- **8:30am – 12:00pm**
  Tutorial I: Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems
  Prof. Krishnendu Chakrabarty, Duke University

- **2:00pm-6:00pm**
  Tutorial II: Statistical Adaptive Test Methods Targeting 'Zero Defect' IC Quality and Reliability
  Prof. Adit D. Singh, Auburn University

Nov. 17

- **8:30am – 9:00am**
  Opening Session
- **9:00am – 10:00am**
  Keynote: Improving Design, Manufacturing, and Even Test through Test-Data Mining
  Prof. Shawn Blanton, Carnegie Mellon University
- **10:00am – 10:30am Coffee break**
- **10:30am – 11:15am**
  Invited talk I: Transformation of DFT: From Load Board to Dashboard
  Mr. Greg Aldrich, Marketing Director at Mentor Graphics
- **11:15am – 12:00pm**
- **Invited talk II: The Characterization Challenges in Modeling Semi-Floating Gate Transistors**
  Prof. David Wei Zhang, Fudan University

- **12:00pm – 1:30pm Lunch**

- **1:30pm – 2:45pm Session 1A/1B/1C**

Session 1A: 3D Testing

Session Chair: Li Jiang, Shanghai Jiao Tong University

- **BIST-Assisted Tuning Scheme for Minimizing IO-Channel Power of TSV-Based 3D DRAMs**

Yun-Chao Yu[1], Chi-Chun Yang[1], Jin-Fu Li[1], Chih-Yen Lo[2], Chao-Hsun Chen[2], Jenn-Shiang Lai[2], Ding-Ming Kwai[2], Yung-Fa Chou[2], and Cheng-Wen Wu[3]

[1]Department of Electrical Engineering National Central University

[2]Information and Communication Research Lab. Industrial Technology Research Institute

[3]Department of Electrical Engineering, National Tsing Hua University

- **Dual-Speed TAM Optimization of 3D SoCs for Mid-Bond and Post-Bond Testing**

Kele Shen[1], Dong Xiang[2] and Zhou Jiang[2]

[1]Department of Computer Science, Tsinghua University

[2]School of Software, Tsinghua University

- **Optimized Pre-bond Test Methodology for Silicon Interposer Testing**

Katherine Shu-Min Li[1], Sying-Jyan Wang[2], Jia-Lin Wu[1], Cheng-You Ho[1], Yingchieh Ho[3], Ruei-Ting Gu[1,4], Bo-Chuan Cheng[4]

[1]Department of Computer Science, National Sun Yat-sen University, Kaohsiung, Taiwan

[2]Department of Computer Science, National Chung Hsing University, Taichung, Taiwan

[3]Department of Electrical Engineering, National Dong Hwa University, Hualien, Taiwan

[4]Advanced Semiconductor Engineering (ASE) Group, Kaohsiung, Taiwan

Session 1B: Reliability

Session Chair: Zhiyuan Wang, Huawei Crop.

- **Design of a Radiation Hardened Latch for Low-power Circuits**

Huaguo Liang[1], Zhi Wang[1], Zhengfeng Huang[1], and Aibin Yan[2]

[1]School of Electronic Science and Applied Physics, Hefei University of Technology, Hefei 230009, P.R. China

[2]School of Computer and Information, Hefei University of Technology, Hefei 230009, P.R. China

- **Optimal Redundancy Designs for CNFET-Based Circuits**

Da Cheng, Fangzhou Wang, Feng Gao, and Sandeep K. Gupta

Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA

- **A Heuristically Mechanical Model for Accurate and Fast Soft Error Analysis**

Jiajia Jiao, Yuzhuo Fu

School of Micro Electronics, Shanghai Jiao Tong University, Shanghai, China

Special Session 1C: Resilient Circuit Design and Test

Moderator: Mehdi Tahoori, Karlsruhe Institute of Technology, Germany

- **Error Resilient Real-Time State Variable Systems for Signal Processing and Control**

Suvadeep Banerjee[1], A´ lvaro Go´mez-Pau[2], Abhijit Chatterjee[1] and Jacob A. Abraham[3]

[1]School of Electrical and Computer Engineering, Georgia Institute of Technology

[2]Universitat Polit`ecnica de Catalunya, Barcelona, Spain

[3]Electrical and Computer Engineering, University of Texas at Austin

- **Variability and Soft-Error Resilience in Dependable VLSI Platform**

Yukio Mitsuyama[1] , and Hidetoshi Onodera[2],

[1]Kochi University of Technology, [2] Kyoto University

- **Adaptive Mitigation of Parameter Variations**

Farshad Firouzi[1], Fangming Ye[2], Saman Kiamehr[1], Krishnendu Chakrabartyz[2], and Mehdi B. Tahooriy[1]

[1]Karlsruhe Institute of Technology, Germany

[2]Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA

- **2:45pm – 3:15pm Coffee break**

- **3:15pm – 4:30pm Session 2A/2B/2C**

Session 2A: Testing of Emerging Technologies

Session Chair: Sandeep Gupta, Univ. of Southern California

- **Reliability-Driven Pipelined Scan-Like Testing of Digital Microfluidic Biochips**

Zipeng Li[1], Trung Anh Dinh[2], Tsung-Yi Ho[3], Krishnendu Chakrabarty[1]

[1]Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA

[2]Graduate School of Information Science and Engineering, Ritsumeikan University, Shiga, Japan

[3]*Computer* Science Department, National Chiao Tung University, Hsinchu, Taiwan

- **A Cost-Effective Stimulus Generator for Battery Channel Characterization in Electric Vehicles**

  Shao-Feng Hung, Long-Yi Lin, and Hao-Chiao Hong

  Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan

- **Generator for Test Set Construction of SMGF in Reversible Circuit by Boolean Difference Method**

  Bappaditya Mondal[1], Dipak Kumar Kole[1], Debesh Kumar Das[2] and Hafizur Rahaman[1]

  [1]Department of Information Technology, Indian Institute of Engineering Science and Technology, Shibpur, India

  [2]Department of Computer Science and Engineering, Jadavpur University, Kolkata, India

Session 2B: SoC Testing

Session Chair: Yu Huang, Mentor Graphics

- **High-Speed Serial Embedded Deterministic Test for System-on-Chip Designs**

  Maciej Trawka Grzegorz Mrugalski[1], Nilanjan Mukherjee[1], Artur Pogiel[2], Janusz Rajski[2]

  Jakub Janicki[3], Jerzy Tyszer[3]

  [1]Gdańsk University of Technology, 80-233 Gdańsk, Poland

  [2]Mentor Graphics Corporation, Wilsonville, OR 97070, USA

  [3]Poznań University of Technology, 60-965 Poznań, Poland

- **A Scalable and Parallel Test Access Strategy for NoC-Based Multicore System**

  Taewoo Han, Inhyuk Choi, Hyunggoy Oh, Sungho Kang

  Department of Electrical and Electronic Engineering, Computer systems & reliable SoC Lab., Yonsei University, Seoul, Korea

- **On Covering Structural Defects in NoCs by Functional Tests**

  Atefe Dalirsani, Nadereh Hatami, Michael E. Imhof, Marcus Eggenberger, Gert Schley,

  Martin Radetzki, Hans-Joachim Wunderlich

  Institute of Computer Architecture and Computer Engineering, University of Stuttgart, Germany

Special Session 2C: Design, Verification and Application of IEEE 1687

Moderator: Erik Larsson, Lund University, Sweden

- **Design, Verification and Application of IEEE 1687**

Farrokh Ghani Zadegan[1], Erik Larsson[1], Artur Jutman[2], Sergei Devadze[2], Rene´ Krenz-Baath[3]

[1]Lund University, Lund, Sweden

[2]Testonica Lab, Tallinn, Estonia

[3]Hochschule Hamm-Lippstadt, Hamm, Germany

- **4:30pm – 5:00pm Coffee break**
- **5:00pm – 6:40pm Session 3A/3B/3C**

Session 3A: Post-Silicon Validation

Session Chair: Michael Hsiao, Virginia Tech.

- **Silicon Evaluation of Cell-Aware ATPG Tests and Small Delay Tests**

Fan Yang[1], Sreejit Chakravarty[1], Arun Gunda[1], Nicole Wu[2] and Jianyu Ning[2]

[1]Avago Technologies, San Jose, CA, USA

[2]Avago Technologies, Shanghai, China

- **On Supporting Sequential Constraints for On-Chip Generation of Post-Silicon Validation Stimuli**

Xiaobing Shi and Nicola Nicolici

Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada

- **Predicting IC Defect Level using Diagnosis**

Cheng Xue and R.D. (Shawn) Blanton

ECE Department, Carnegie Mellon University, Pittsburgh, PA, USA

Session 3B: Testability and Test Generation

Session Chair: Hans-Joachim Wunderlich, University of Stuttgart

- **Testability-Driven Fault Sampling for Deterministic Test Coverage Estimation of Large Designs**

Kun-Han Tsai

Mentor Graphics Corporation, Wilsonville, OR 97070, USA

- **Methodology for Early RTL Testability and Coverage Analysis and Its Application to Industrial Designs**

Chandan Kumar[1], Fadi Maamari[1], Kiran Vittal[1], Wilson Pradeep[2], Rajesh Tiwari[2], Srivaths Ravi[2]

[1]Atrenta Inc., San Jose, U.S.A

[2]Texas Instruments Inc., Bengaluru, India

- **Circuit Parameter Independent Test Pattern Generation for Interconnect Open Defects**

Dominik Erb[1], Karsten Scheibler[1], Matthias Sauer[1], Sudhakar M. Reddy[2], Bernd Becker[1]

[1]Chair of Computer Architecture, University of Freiburg, Germany

[2]Dept. of ECE, University of Iowa, USA

Session 3C: TTTC's Doctoral Thesis Award: Asian Semi-Final

Session Chair: Jiun-Lang Huang, National Taiwan University

- **Researching on the critical techniques of metamorphic testing to provide more effective test oracle**

Zhan-Wei Hui,

PLA Univ. of Science and Technology

- **Yield and reliability enhancement for 3D ICs**

Li Jiang,

The Chinese University of Hong Kong

- **An analytical model driven framework for accurate and efficient soft error analysis in processors**

Jiajia Jiao,

Shanghai Jiao Tong University

- **Diagnosis techniques for identifying faults in digital VLSI system**

Subhadip Kundu,

IIT Kharagpur

- **Multiple-fault-oriented fault diagnosis for digital integrated circuits**

Jing Ye,

Institute of Computing Technology, Chinese Academy of Sciences

Nov. 18

- **9:00am – 10:15am Session 4A/4B/4C**

Session 4A: Yield Optimization of Memory

Session Chair: Jin-Fu Li, National Central University

- **Built-In Scrambling Analysis for Yield Enhancement of Embedded Memories**

Shyue-Kung Lu[1], Hao-Cheng Jheng[1], Hao-Wei Lin[1], Masaki Hashizume[2], and Seiji Kajihara[3]

[1]Dept. Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan

[2] Institute of Technology and Science, The University of Tokushima, Tokushima, Japan

[3]Dept. Creative Informatics, Kyushu Institute of Technology, Kyushu, Japan

- **Intra-Channel Reconfigurable Interface for TSV and Micro Bump Fault Tolerance in 3-D RAMs**

Kuan-Te Wu[1], Jin-Fu Li[1], Yun-Chao Yu[1], Chih-Sheng Hou[1], and Chi-Chun Yang[1], Ding-Ming Kwai[2], Yung-Fa Chou[2] and Chih-Yen Lo[2]

[1]Department of Electrical Engineering, National Central University, Taoyuan, Taiwan 320

[2]Information and Communication Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan 310

- **SRAM array yield Estimation under spatially-correlated process variation**

Jizhe Zhang and Sandeep Gupta

Department of Electrical Engineering, University of Southern California

Session 4B: On-Line Parameter Testing

Session Chair: Xiaoxiao Wang, Beihang University

- **Temperature and Voltage Estimation Using Ring-Oscillator-Based Monitor for Field Test**

Yousuke Miyake[1], Yasuo Sato[1], Seiji Kajihara[1]and YukiyaMiura[2]

[1]Kyushu Institute of Technology, Iizuka, Japan

[2]Tokyo Metropolitan University, Tokyo, Japan

- **On-Line Transition-Time Monitoring for Die-to-Die Interconnects in 3D ICs**

Shi-Yu Huang[1], Hua-Xuan Li[1], Zeng-Fu Zeng[1], Kun-Han Tsai[2], and Wu-Tung Cheng[2]

[1]Electrical Engineering Department, National Tsing Hua University, Taiwan

[2]Silicon Test Solutions, Mentor Graphics

- **A Novel Circuit for Transition-Edge Detection: Using a Stochastic Comparator Group to Test Transition-Edge**

Takahiro J. Yamaguchi[1,3], James S. Tandon[2,3], Satoshi Komatsu[3,4], Kunihiro Asada[3]

[1]Advantest Laboratories, Ltd., Sendai, Miyagi, Japan

[2]Microsemi, San Jose, CA, USA

[3]D2T, VDEC, The University of Tokyo, Tokyo, Japan

[4]School of Engineering, Tokyo Denki University, Tokyo, Japan

Session 4C: Embedded Tutorial-Hierarchical Scan Compression 1

Yu Huang, Mentor Graphics

ZhenXin Sun, Cadence

Ang Li, Synopsys

- **10:15am – 10:45am Coffee break**
- **10:45am – 12:00pm Session 5A/5B/5C**

Session 5A: Power/Temperature-Aware Testing

Session Chair: Seiji Kajihara, Kyushu Institute of Technology

- **Low Power Test Compression with Programmable Broadcast-Based Control**

Sylwester Milewski[1], Grzegorz Mrugalski[2], Janusz Rajski[2], Jerzy Tyszer[1]

[1]Poznań University of Technology, 60-965 Poznań, Poland

[2]Mentor Graphics Corporation, Wilsonville, OR 97070, USA

- **Exploit Dynamic Voltage and Frequency Scaling for SoC Test Scheduling under Thermal Constraints**

Li Ling, Jianhui Jiang

School of Software Engineering, Tongji University, Shanghai, China

- **High Quality Testing of Grid Style Power Gating**

Vasileios Tenentes[1], Saqib Khursheed[2], Bashir M. Al-Hashimi[1], Shida Zhong[1], Sheng Yang[1]

[1]ECS, University of Southampton, UK.

[2]Electrical Engineering & Electronics, University of Liverpool, UK.

Session 5B: Trojan/Fault Detection with High Resolution

Session Chair: Katherine Shu-Min Li, National Sun Yat-Sen University

- **A Resizing Method to Minimize Effects of Hardware Trojans**

Byeongju Cha and Sandeep K. Gupta

Ming Hsieh Department of Electrical Engineering, University of Southern California Los Angeles, USA

- **High Resolution Pulse Propagation Driven Trojan Detection In Digital Logic: Optimization Algorithms and Infrastructure**

Sabyasachi Deyati[1] ,Barry John Muldrey[1], Adit Singh[2], Abhijit Chatterjee[1]

[1]Electrical & Computer Engineering, Georgia Institute of Technology, Atlanta GA 30332, USA

[2]Department of Electrical Engineering, Auburn University, AL 36849, USA

- **Physically-Aware Diagnostic Resolution**

John A. Porche, R. D. (Shawn) Blanton

Dept. of ECE Carnegie Mellon University Pittsburgh, PA 15213

Session 5C: Embedded Tutorial- Hierarchical Scan Compression 2

Yu Huang, Mentor Graphics

ZhenXin Sun, Cadence

Ang Li, Synopsys

- **12:00pm – 1:30pm Lunch**

- **1:30pm – 3:10pm Session 6A/6B/6C**

Session 6A: Analog/Memory Testing

Session Chair: Jiun-Lang Huang, National Taiwan University

- **On-chip implementation of an Integrator-Based servo-loop for ADC static linearity test**

Guillaume Renaud[1], Manuel J. Barragan[1], and Salvador Mir[1], Marc Sabut[2]

[1]Universite Grenoble Alpes, TIMA, F-38000 Grenoble, France ´ CNRS, TIMA, F-38000 Grenoble, France

[2]STMicroelectronics Grenoble 12, Rue Jules Horowitz, F-38000 Grenoble, France

- **An ATE Based 32 Gbaud PAM-4 At-Speed Characterization and Testing Solution**

Jose Moreira[1], Hubert Werkmann[1], Masahiro Ishida[1], Bernhard Roth[1], Volker Filsinger[2], Sui-Xia Yang[1]

[1]Advantest

[2]SHF Communication Technologies

- **Testing of Non-Volatile Logic-Based System Chips**

Yong-Xiao Chen and Jin-Fu Li

Advanced Reliable Systems (ARES) Lab, Department of Electrical Engineering, National Central University, Jhongli, Taiwan 320

- **Dual-Purpose Mixed-Level Test Generation Using Swarm Intelligence**

Kelson Gent and Michael S. Hsiao

Bradley Department of Electrical and Computer Engineering Virginia Tech, Blacksburg, VA 24061, USA

Panel Session 6B: Big Data for Test

Moderators: K.-T. Tim Cheng, University of California, Santa Barbara
Harry H. Chen, MediaTek Inc.

- **Learning from Production Test Data: Correlation Exploration and Feature Engineering**

Fan Lin, Chun-Kai Hsu, and Kwang-Ting Cheng

Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106

- **Leveraging Big Data Analytics to Drive Failure Analysis in Manufacturing Operations**

David Park,

Optimal+

- **Data Driven Design Centric Yield Learning**

John Kim,

Synopsys

- **Perspectives on Test Data Mining from Industrial Experience**

Harry H. Chen,

Design Technology Department, MediaTek Inc. Hsinchu, Taiwan

Special Session 6C: In-Field Techniques for Performance Adaption, Test, and Power-Noise Diagnosis

Moderator: Xiaoqing Wen, Kyushu Institute of Technology, Japan

- **Opportunities and Verification Challenges of Run-time Performance Adaptation**

Masanori Hashimoto

Dept. Information Systems Engineering, Osaka University

- **An On-Chip Digital Environment Monitor for Field Test**

Seiji Kajihara, Yousuke Miyake, Yasuo Sato, Yukiya Miura(

Kyushu Institute of Technology

- **On-Chip Monitoring for In-Place Diagnosis of Undesired Power Domain Problems in IC Chips**

Makoto Nagata, Daisuke Fujimoto, Noriyuki Miura

Graduate School of System Informatics, Kobe University, Japan

- **3:30pm – 10:00pm Social Event & Banquet**

Nov. 19

- **9:00am – 10:15am Session 7A/7B/7C**

Session 7A: Timing Variation Detection

Session Chair: Shi-Yu Huang, National Tsinghua University

- **An On-Line Timing Error Detection Method for Silicon Debug**

Yun Cheng[1,2], Huawei Li[1], Xiaowei Li[1]

[1]State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

[2]University of Chinese Academy of Sciences, Beijing, China

- **An All Digital Distributed Sensor Network Based Framework for Continuous Noise Monitoring and Timing Failure Analysis in SoCs**

Mehdi Sadi [1], Zoe Conroy [2], Bill Eklow [2], Matthias Kamm [2], Nematollah Bidokhti [2] and Mark (Mohammad) Tehranipoor [1]

[1]Dept. of Electrical & Computer Engineering, University of Connecticut, Storrs, USA

[2]Cisco Systems, San Jose, CA, USA

- **On-Chip Delay Sensor for Environments with large Temperature Fluctuations**

Jibing Qiu, Guihai Yan, Xiaowei Li

State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

Session 7B: Delay Testing

Session Chair: Bernd Becker, University of Freiburg

- **Timing Evaluation Tests for Scan Enable Signals with Application to TDF Testing**

Jie Zou, Chao Han and Adit D. Singh

Department of Electrical and Computer Engineering, Auburn University, Auburn AL, 36849

- **FPGA-Based Subset Sum Delay Lines**

Chung-Yun Wang[1], Yu-Yi Chen[1], Jiun-Lang Huang[1], Xuan-Lun Huang[2]

[1]Graduate Institute of Electronics Engineering, Department of Electrical Engineering, National Taiwan University

[2]Industrial Technology Research Institute, Hsinchu, Taiwan

- **Parallel Path Delay Fault Simulation for Multi/Many-Core Processors with SIMD Units**

Yussuf Ali[1] Yuta Yamato[1] Tomokazu Yoneda[1] Kazumi Hatayama[2] Michiko Inoue[1]

[1] Nara Institute of Science and Technology, Nara, Japan

[2]Gunma University, Gunma, Japan

Special Session 7C: High Quality System Level Test and Diagnosis

Moderator: Hans-Joachim Wunderlich, University of Stuttgart

- **High Quality System Level Test and Diagnosis**

Artur Jutman[1], Matteo Sonza Reorda[2], Hans-Joachim Wunderlich[3]

[1]Testonica Lab, Tallinn, Estonia, [2]Politecnico di Torino, Italy, [3]University of Stuttgart, Germany

- **10:15am – 10:45am Coffee break**

- **10:45am – 12:00pm Session 8A/8B/8C**

Session 8A: Diagnosis

Session Chair: Sybille Hellebrand, University of Paderborn

- **An Efficient Diagnosis Pattern Generation Procedure to Distinguish Stuck-at Faults and Bridging Faults**

Cheng-Hung Wu and Kuen-Jong Lee

Dept. of EE, National Cheng Kung University, Taiwan

- **On the Generation of Diagnostic Test Set for Intra-cell Defects**

Z. Sun[1], A. Bosio[1], L. Dilillo[1], P. Girard[1], A. Virazel[1], E. Auvray[2]

[1]LIRMM UM2-CNRS, Montpellier, France

[2]ST Microelectronics, Grenoble, France

- **Diagnosing Cell Internal Defects Using Analog Simulation-based Fault Models**

Huaxing Tang[1], Brady Benware[1], Michael Reese[2], Joseph Caroselli[2], Thomas Herrmann[3], Friedrich Hapke[4], Robert Tao[2], Wu-Tung Cheng[1], Manish Sharma[1]

[1]Mentor Graphics, Wilsonville, Oregon, USA

[2]AMD, Inc. Austin, Texas, USA

[3]GLOBALFOUNDRIES, Dresden, Germany

[4]Mentor Graphics, Hamburg, Germany

Session 8B: Test Compression

Session Chair: Huaguo Liang, Hefei University of Technology

- **Improving Output Compaction Efficiency with High Observability Scan Chains**

Sying-Jyan Wang[1], Che-Wei Kao[1], Katherine Shu-Min Li[2]

[1]Department of Computer Science and Engineering, National Chung Hsing University, Taichung, Taiwan

[2]Department of Computer Science and Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

- **Two-Step Dynamic Encoding for Linear Decompressors**

Emil Gizdarski

Synopsys Inc., 700 East Middlefield Road, Mountain View, CA 94043

- **A Case Study on Implementing Compressed DFT Architecture**

A. Chandra, S. Chebiyam, and R. Kapur

Synopsys, Inc., 700 E. Middlefield Rd., Mountain View, CA, 94043, USA

Special Session 8C: Hardware Security

Moderator: Yier Jin, University of Central Florida

- **Leveraging Emerging Technology for Hardware Security - Case Study on Silicon Nanowire FETs and Graphene SymFETs**

Yu Bi[1], Pierre-Emmanuel Gaillardon[2], X. Sharon Huz[3], Michael Niemierz[3], Jiann-Shiun Yuan[1], and Yier Jin[1]

[1]Department of Electrical Engineering and Computer Science, University of Central Florida

[2]Ecole Polytechnique F ´ ed´ erale de Lausanne (EPFL) - Switzerland ´

[3]Department of Computer Science and Engineering, University of Notre Dame

- **Advanced Analysis of Cell Stability for Reliable SRAM PUFs**

Alison Hosey, Md. Tauhidur Rahman, Kan Xiao, Domenic Forte, and Mohammad Tehranipoor

ECE Department, University of Connecticut

- **On the Use of Scan Chain to Improve Physical Attacks**

Junfeng Fan[1], Hua Xie[2], Yiwei Zhang[2]

[1]Nationz technologies and Open Security Research, Shenzhen, China

[2]Nationz technologies, Shenzhen, China