2013 Asian Test Symposium Program

Nov. 18, 2013 (Monday)

Time	Session	Details
10:00 - 12:30	**Tutorial I (Pine Room)**	**Statistical Adaptive Test Methods Targeting "Zero Defect" IC Quality and Reliability - (1/2)**
		Prof. Adit D. Singh, Dept. of Electrical and Computer Engineering, Auburn University
	Tutorial II (Peak Room)	**Testing TSV-Based 3D Stacked ICs - (1/2)**
		Prof. Krishnendu Chakrabarty, Dept. of Electrical and Computer Engineering,
12:30 - 13:30	**Lunch**	
13:30 - 17:30	**Tutorial I (Pine Room)**	**Statistical Adaptive Test Methods Targeting "Zero Defect" IC Quality and Reliability - (2/2)**
		Prof. Adit D. Singh, Dept. of Electrical and Computer Engineering, Auburn University
	Tutorial II (Peak Room)	**Testing TSV-Based 3D Stacked ICs - (2/2)**
		Prof. Krishnendu Chakrabarty, Dept. of Electrical and Computer Engineering,
	Advance Registration	
18:30 -	**ATS'13 Reception (Evergreen Room I)**	

Nov. 19, 2013 (Tuesday)

Time	Session	Details
07:40 - 08:35	**Registration**	
08:35 - 08:50	**Opening**	
08:50 - 09:50	**Keynote (Evergreen Room I)**	**Test Data Analytics - from Mathematical Tools to Applications** Chair: Dr. Chen-Wen Wu, ITRI
		Prof. Kwang-Ting Cheng (UC Santa Barbara)
09:50 - 10:20	**Coffee Break**	
10:20 - 11:10	**Invited Talk I (Evergreen Room I)**	**New Approaches to Improving Quality and Accelerating Yield Ramp to Meet Process Technology Disruptions** Chair: Prof. Shi-Yu Huang, National Tsing Hua University
		Dr. Wu-Tung Cheng (Mentor Graphics)
11:10 - 12:00	**Invited Talk II (Evergreen Room I)**	**3DIC's System Design Impact and Testing Needs** Chair: Prof. Sying-Jyan Wang, National Chung Hsing University
		Dr. William Wu Shen (TSMC)
12:00 - 13:30	**Lunch**	
13:30 - 14:45	**Session 4A (Pine Room)**	**3D-IC Design-for-Test** Chair: Shu-Min LI (National Sun Yat-sen University)
		* Exploration Methodology for 3D Memory Redundancy Architectures under Redundancy Constraints
		Bing-Yang LIN (National Tsing Hua University), Mincent LEE (National Tsing Hua University), Cheng-Wen WU (National Tsing Hua University)
		* A TSV Repair Scheme Using Enhanced Test Access Architecture for 3-D ICs

Chi-Chun YANG (Natioanl Central University), Che-Wei CHOU (National Central University), Jin-Fu LI (National Central University)

* Testable Design for Electrical Testing of Open Defects at Interconnects in

Masaki HASHIZUME (University of Tokushima), Tomoaki KONISHI (University of Tokushima), Hiroyuki YOTSUYANAGI (University of Tokushima), Shyue-Kung LU (National Taiwan Univ. of Science and

Session 4B (Peak Room)	**Power/Thermal Aware Testing I** Chair: Kohei MIYASE (Kyushu Institute of Technology)

* On Achieving Capture Power Safety in At-Speed Scan-Based Logic BIST

Akihiro TOMITA (Kyushu Institute of Technology), Xiaoqing WEN (Kyushu Institute of Technology), Yasuo SATO (Kyusyu Institute of Technology), Seiji KAJIHARA (Kyushu Institute of Technology), Patrick GIRARD (LIRMM), Mohammad TEHRANIPOOR (University of Connecticut), Laung-Terng WANG (SynTest Technologies, Inc.)

* Thermal Aware Don't Care Filling to Reduce Peak Temperature and Thermal Variance during Testing

Arpita DUTTA (IIT Kharagpur), Subhadip KUNDU (IIT Kharagpur), Santanu CHATTOPADHYAY (IIT Kharagpur)

* Peak Capture Power Reduction for Compact Test Sets Using Opt-Justification-Fill

Stephan EGGERSGLUESS (University of Bremen/DFKI)

Session 4C (River Room)	**Embedded Tutorial I: Data Mining in Test - Principles and Practices (Part I)** Chair: Hung-Pin WEN (National Chiao Tung University)

Prof. Li-C Wang (UC Santa Barbara)

14:45 - 15:15	**Coffee Break**	
15:15 - 16:30	**Session 5A (Pine Room)**	**At-Speed Testing** Chair: Yi-Shing CHANG (Intel)

* Worst-Case Critical-Path Delay Analysis Considering Power-Supply Noise

Fang BAO (University of Connecticut), Harry CHEN (MediaTek Inc.), Mohammad TEHRANIPOOR (University of Connecticut)

* Test Generation of Path Delay Faults Induced by Defects in Power TSV

Chi-Jih SHIH (National Taiwan University), Shih-An HSIEH (National Taiwan University), Yi-Chang LU (National Taiwan University), James C.-M. LI (National Taiwan University), Tzong-Lin WU (National Taiwan University), Krishnendu CHAKRABARTY (Duke University)

* Multicycle-Aware At-Speed Test Methodology

Kun-Han TSAI (Mentor Graphics Corp.), Xijiang LIN (Mentor Graphics Corp.)

Session 5B (Peak Room)	**Analog/Mixed-Signal Test** Chair: Soon-Jyh CHANG (National Cheng Kung University)

* Analog Sensor Based Testing of Phase-Locked Loop Dynamic Performance Parameters

Sen-Wen HSIAO (Georgia Institute of Technology), Xian WANG (Georgia Institute of Technology), Abhijit CHATTERJEE (Georgia Institute of

* Built-In Test of Switched-Mode Power Converters: Avoiding DUT Damage Using Alternative Safe Measurements

Xian WANG (Georgia institute of technology), Blanchard KENFACT (Texas Instruments), Estella SILVA (Texas Instruments), Abhijit CHATTERJEE (Georgia Institute of Technology)

* Design of a Fault-Injectable Fleischer-Laker Switched-Capacitor Biquad for verifying the Static Linear Behavior Fault Model

Long-Yi LIN (National Chiao Tung University), Hao-Chiao HONG (National Chiao Tung University)

	Session 5C (River Room)	**Embedded Tutorial I: Data Mining in Test - Principles and Practices (Part II)** **Chair: Hung-Pin WEN (National Chiao Tung University)**
		Prof. Li-C Wang (UC Santa Barbara)
16:30 - 17:00	**Break**	
17:00 - 18:15	**Session 6A (Pine Room)**	**Diagnosis and Debug** **Chair: Kun-Han TSAI (Mentor Graphics)**

* Failure Localization of Logic Circuits Using Voltage Contrast Considering State of Transistors

Masafumi NIKAIDO (Renesas Electronics Corp.), Yukihisa FUNATSU (Renesas Electronics Corp.), Tetsuya SEIYAMA (Renesas Electronics Corp.), Junpei NONAKA (Renesas Electronics Corp.), Kazuki SHIGETA (Renesas

* Handling Missing Syndromes in Board-Level Functional-Fault Diagnosis

Fangming YE (Duke University), Shi JIN (Duke University), Zhaobo ZHANG (Huawei Technologies), Krishnendu CHAKRABARTY (Duke University), Xinli GU (Huawei Technologies)

* Diagnosing Resistive Open Faults Using Small Delay Fault Simulation

Koji YAMAZAKI (Meiji University), Toshiyuki TSUTSUMI (Meiji University), Hiroshi TAKAHASHI (Ehime University), Yoshinobu HIGAMI (Ehime University), Hironobu YOTSUYANAGI (University of Tokushima), Masaki HASHIZUME (University of Tokushima), Kewal K. SALUJA (University of

Session 6B (Peak Room)	**Design-for-Test I** **Chair: Chia-Tso CHAO (National Chiao Tung University)**

* A Transient Fault Tolerant Test Pattern Generator for On-line Built-in Self-

Yuki FUKAZAWA (Hiroshima City University), Tsuyoshi IWAGAKI (Hiroshima City University), Hideyuki ICHIHARA (Hiroshima City University), Tomoo INOUE (Hiroshima City Uniersity)

* Leakage Monitoring Technique in Near-threshold Systems with a Time-based Bootstrapped Ring Oscillator

Yingchieh HO (National Dong-Hwa University), Katherine Shu-Min LI (National Sun Yat-sen University), Sying-Jyan WANG (National Chung-

* A New LFSR Reseeding Scheme via Internal Response Feedback

Wei-Cheng LIEN (National Cheng Kung University), Kuen-Jong LEE (National Cheng Kung Univ), Tong-Yu HSIEH (National Sun Yat-sen University), Krishnendu CHAKRABARTY (Duke University)

Session 6C (River Room)	**Industry Session I** **Chair: Chun-Lung HSU (Industrial Technology Research Institute)**

* Automotive EEPROM qualification and cost optimisation

Pete SARSON (ams AG), Gregor SCHATZBERGER (ams AG), Robert SEITZ

* Cost-Effective TAP-Controlled Serialized Compressed Scan Architecture for 3D Stacked ICs

Chen-An CHEN (ITRI), Yee-Wen CHEN(ITRI), Chun-Lung HSU (ITRI), Ming-Hsueh WU (ITRI), Kun-Lun LUO (ITRI), Bing-Chuan BAI (ITRI), Liang-Chia

Nov. 20, 2013 (Wednesday)

08:30 - 09:45

Session 7A (Pine Room) — **Memory Defects**
Chair: Shi-Yu HUANG (National Tsing Hua University)

* Adaptive Source Bias for Improved Resistive-Open Defect Coverage during SRAM Testing
  Elena Ioana VATAJELU (LIRMM), Luigi DILILLO (LIRMM), Alberto BOSIO (LIRMM), Patrick GIRARD (LIRMM), Aida TODRI-SANIAL (CNRS-LIRMM), Arnaud VIRAZEL (LIRMM), Nabil BADEREDDINE (Intel Mobile
* A New March Test for Process-Variation Induced Delay Faults in SRAMs
  Da CHENG (University of Southern California), Hsunwei HSIUNG (University of Southern California), Bin LIU (University of Southern California), Sandeep GUPTA (University of Southern California)
* Back-End-of-Line Defect Analysis for Rnv8T Nonvolatile SRAM
  Bing-Chuan BAI (ITRI), James C.-M. LI (National Taiwan University), Kun-Lun LUO (ITRI), Chen-An CHEN (ITRI), Yee-Wen CHEN (ITRI), Ming-Hsueh WU (ITRI), Chun-Lung HSU (ITRI), Liang-Chia CHENG (ITRI)

Session 7B (Peak Room) — **Converter Testing**
Chair: Hao-Chiao HONG (National Chiao Tung University)

* Digital Calibration for 8-bit Delay Line ADC Using Harmonic Distortion Correction
  Hsun-Cheng LEE (University of Texas at Austin), Jacob A. ABRAHAM (University of Texas at Austin)
* Digital Compensation for Timing Mismatches in Interleaved ADCs
  Ru YI (Gunma University), Minghui WU (Gunma University), Koji ASAMI (Advantest Corp.), Haruo KOBAYASHI (Gunma University), Ramin KHATAMI (Gunma University), Atsuhiro KATAYAMA (Gunma University), Isao SHIMIZU (Gunma University), Kentaroh KATOH (Tsuruoka National College
* An Analysis of Stochastic Self-Calibration of TDC Using Two Ring Oscillators
  Kentaroh KATOH (Tsuruoka National College of Technology), Yuta DOI (Gunma University), Satoshi ITO (Gunma University), Haruo KOBAYASHI (Gunma University), Ensi LI (Gunma University), Nobukazu TAKAI (Gunma University), Osamu KOBAYASHI (STARC)

Session 7C (River Room) — **Embedded Tutorial II: Soware Testing**
Chair: Stefan HOLST (Kyushu Institute of Technology)

Prof. Farn Wang (National Taiwan University)

09:45 - 10:15 **Coffee Break**

10:15 - 11:30

Session 8A (Pine Room) — **3D-IC Interposer Test**
Chair: Tong-Yu HSIEH (National Sun Yat-sen University)

* Post-Bond Testing of the Silicon Interposer and Micro-Bumps in 2.5D ICs
  Ran WANG (Duke University), Krishnendu CHAKRABARTY (Duke University), Bill EKLOW (Cisco Systems, Inc.)
* Mid-bond Interposer Wire Test

Li-Ren HUANG (National Tsing Hua University), Shi-Yu HUANG (National Tsing-Hua University), Kun-Han TSAI (Mentor Graphics Corp.), Wu-Tung CHENG (Mentor Graphics Corp.), Stephen SUNTER (Mentor Graphics Corp.)

* A Layout-Aware Test Methodology for Silicon Interposer in System-in-a-

Katherine Shu-Min LI (National Sun Yat-sen University), Cheng-You HO (National Sun Yat-sen University), Ruei-Ting GU (National Sun Yat-sen University/ASE), Sying-Jyan WANG (National Chung-Hsing University), Yingchieh HO (National Dong Hwa University), Jiun-Jie HUANG (ASE), Bo-Chuan Cheng (ASE), An-Ting LIU (ASE)

	Session 8B (Peak Room)	**Power/Thermal Aware Testing II Chair: Shu-Min LI (National Sun Yat-sen University)**

* Formulating Optimal Test Scheduling Problem with Dynamic Voltage and Frequency Scaling

Spencer K. MILLICAN (University of Wisconsin - Madison), Kewal K. SALUJA (University of Wisconsin - Madison)

* Search Space Reduction for Low-Power Test Generation

Kohei MIYASE (Kyushu Institute of Technology), Matthias SAUER (University of Freiburg), Bernd BECKER (University of Freiburg), Xiaoqing WEN (Kyushu Institute of Technology), Seiji KAJIHARA (Kyushu Institute of

* MIRID: Mixed-Mode IR-Drop Induced Delay Simulator

Jie JIANG (University of Passau), Marina APARICIO (LIRMM - Univ. of Montpellier), Mariane COMTE (LIRMM - Univ. of Montpellier), Florence AZAIS (LIRMM - Univ. of Montpellier), M. RENOVELL (LIRMM - Univ. of Montpellier), Ilia POLIAN (University of Passau)

	Session 8C (River Room)	**Vendor Sessions: New Test Technologies & Roadmap Chair: Jing-Jia LIOU (National Tsing Hua Univesity)**

* DfT Technologies for High-Quality Cost-Effective Test of SoCs

Janusz Rajski, Mentor Graphics Corp.

* Flexible Test Methodologies for large SoCs

Yi Wang, Cadence Design Systems, Inc.

* New Solutions for Reducing the Time, Effort and Cost of Quality SoC

Mark Lin, Synopsys, Inc.

11:30 - 11:45	**Break**	
11:45 - 13:00	**Session 9A (Pine Room)**	**Defect-Based Test Chair: Michael HSIAO (Virginia Tech)**

* A Stochastic Model for NBTI-Induced LSI Degradation in Field

Yasuo SATO (Kyusyu Institute of Technology), Seiji KAJIHARA (Kyushu Institute of Technology)

* Hazard Initialized LOC Tests for TDF Undetectable CMOS Open Defects

Chao HAN (Auburn University), Adit D. SINGH (Auburn University)

	Session 9B (Peak Room)	**Design-for-Test II Chair: Tomokazu YONEDA (Nara Institute of Science and Technology)**

* Single Test Clock with Programmable Clock Enable Constraints for Multi-Clock Domain SoC ATPG Testing

Chin Hai ANG (Altera Corporation (M) Sdn Bhd)

* On the Generation of Compact Deterministic Test Sets for BIST Ready

Amit KUMAR (University of Iowa), Janusz RAJSKI (Mentor Graphics Corp.), Sudhakar M. REDDY (University of Iowa), Thomas RINDERKNECHT (Mentor Graphics Corp.)

* A Cost-Effective Scheme for Network-on-Chip Router and Interconnect

  Dong XIANG (Tsinghua University)

Session 9C (River Room) | **Industry Session II**
Chair: Hideyuki ICHIHARA (Hiroshima City University)

* External Loopback Testing on High Speed Serial Interface

  Shen Shen LEE (Altera Corporation), Tze Sin TAN (Altera Corporation), Wee Sun VOON (Altera Corporation)

* Multi-Histogram ADC BIST System for ADC Linearity Testing

  Koay Soon CHAN (Marvell Semiconductor Sdn. Bhd.), Nuzrul Fahmi NORDIN (Marvell Semiconductor Sdn. Bhd.), Kim Chon CHAN (Marvell Semiconductor Sdn. Bhd.), Terk Zyou LOK (Marvell Semiconductor Sdn. Bhd.), Chee Wai YONG (Marvell Semiconductor Sdn. Bhd.)

13:00 - 14:30 **Lunch**

14:30 - 17:30 **Social Event**

18:30 - 21:30 **Banquet (Evergreen Room I)**

Nov. 21, 2013 (Thursday)

09:00 - 10:15 **Session 10A (Pine Room)** | **Memory Testing**
Chair: Chien-Mo LI (National Taiwan University)

* Fault Scrambling Techniques for Yield Enhancement of Embedded

  Shyue-Kung LU (National Taiwan Univ. of Science and Technology), Hao-Cheng JHENG (National Taiwan Univ. of Science and Technology), Masaki HASHIZUME (The Univ. of Tokushima), Jiun-Lang HUANG (National Taiwan University), Pony NING (Nanya Technology Corp.)

* Testing Disturbance Faults in Various NAND Flash Memories

  Chih-Sheng HOU (National Central University), Jin-Fu LI (National Central University)

* An efficient method for the test of embedded memory cores during the operational phase

  Paolo BERNARDI (Politecnico Di Torino), Lyl CIGANDA (Politecnico di Torino), Matteo SONZA REORDA (Politecnico Di Torino), Said HAMDIOUI (Delft University of Technology)

Session 10B (Peak Room) | **Automatic Test Pattern Generation**
Chair: Virendra SINGH (Indian Institute of Technology Bombay)

* Functional Test Generation at the RTL Using Swarm Intelligence and Bounded Model Checking

  Kelson GENT (Virginia Tech.), Michael S. HSIAO (Virginia Tech)

* Path Constraint Solving based Test Generation for Hard-to-reach States

  Yanhong ZHOU (Chinese Academy of Sciences), Tiancheng WANG (Chinese Academy of Sciences), Tao LV (Chinese Academy of Sciences), HUAWEI LI (Chinese Academy of Sciences), Xiaowei LI (Chinese Academy of Sciences)

* Accurate Multi-Cycle ATPG in Presence of X-Values

Dominik ERB (University of Freiburg), Michael KOCHTE (University of Stuttgart), Matthias SAUER (University of Freiburg), Hans-Joachim WUNDERLICH ((University of Stuttgart), Bernd BECKER (University of

10:15 - 10:45 **Coffee Break**

10:45 - 12:00

Session 11A (Pine Room)	**Process Variations Chair: Shyue-Kung LU (National Taiwan Univ. of Science and Technology)**

* Interplay of Failure Rate, Perfromance, and Test Cost in TCAM under Process Variations

Hsunwei HSIUNG (University of Southern California), Da CHENG (University of Southern California), Bin LIU (University of Southern California), Ramesh GOVINDAN (University of Southern California), Sandeep K. GUPTA (University of Southern California)

* Critical Paths Selection and Test Cost Reduction Considering Process Variations

Jifeng CHEN (University of Connecticut), Mohammad TEHRANIPOOR (University of Connecticut)

* A Region-Based Framework for Design Feature Identification of Systematic Process Variations

Shuo-You HSU (National Tsing Hua University), Chih-Hsiang HSU (National Tsing Hua University), Ting-Shou HSU (National Tsing Hua University), Jing-Jia LIOU (National Tsing Hua University)

Session 11B (Peak Room)	**High-Speed I/O Testing Chair: Haruo KOBAYASHI (Gunma University)**

* An Active Test Fixture Approach for 40 Gbps and Above At-Speed Testing Using a Standard ATE System

Jose MOREIRA (Advantest), Bernhard ROTH (Advantest), Hubert WERKMANN (Advantest), Lars KLAPPROTH (SHF), Michael HOWIESON (TFT), Mark BROMAN (TFT), Wend OUEDRAOGO (TFT), Mitchell LIN

* Enhanced Resolution Time-domain Reflectometry for High Speed Channels: Characterizing Spatial Discontinuities with Non-ideal Stimulus

Suvadeep BANERJEE (Georgia Institute of Technology), Hyun Woo CHOI (Georgia Institute of Technology), David C. Keezer (Georgia Institute of Technology), Abhijit CHATTERJEE (Georgia Institute of Technology)

* Time Domain Reconstruction of Incoherently Undersampled Periodic Waveforms Using Bandwidth Interleaving

Debesh BHATTA (Georgia Institute of Technology), Nicholas TZOU (Georgia Institute of Technology), Sen-Wen HSIAO (Georgia Institute of Technology), Abhijit CHATTERJEE (Georgia Institute of Technology)

Session 11C (River Room)	**Yield Enhancement and Security Chair: Hiroyuki YOTSUYANAGI (University of Tokushima)**

* An Efficient Test Methodology for Image Processing Applications Based on Error-Tolerance

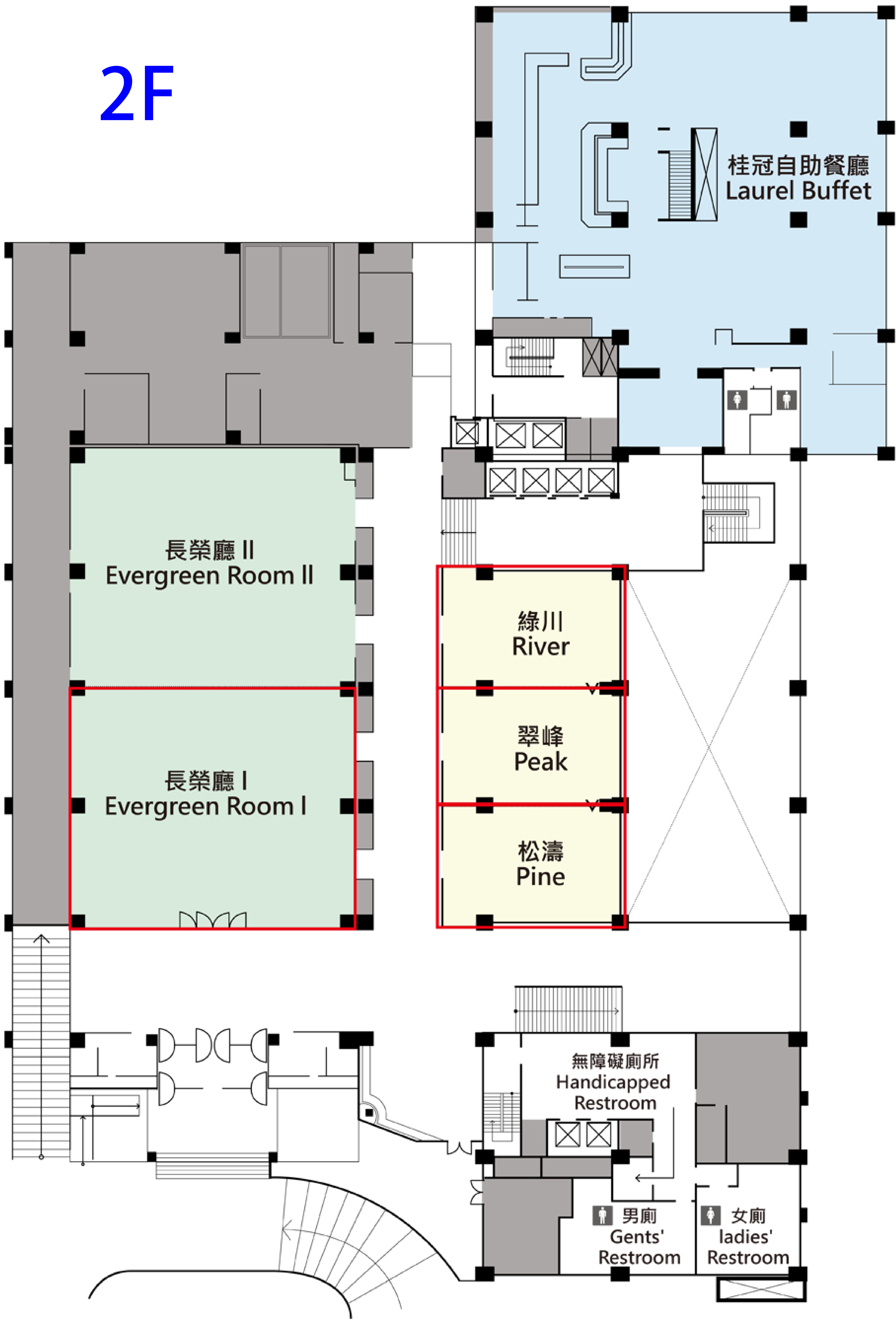
Tong-Yu HSIEH (National Sun Yat-sen University), Yi-Han PENG (National Sun Yat-sen University), Chia-Chi KU (National Sun Yat-sen University)

* Securing Access to Reconfigurable Scan Networks

Rafal BARANOWSKI (University of Stuttgart), Michael A. KOCHTE (University of Stuttgart), Hans-Joachim WUNDERLICH (Universitat

* A Die Selection and Matching Method with Two Stages for Yield Enhancement of 3-D Memories

Wooheon KANG (Yonsei University), Changwook LEE (Yonsei University), Keewon CHO (Yonsei Univesristy), Sungho KANG (Yonsei University)


2F
桂冠自助餐廳
Laurel Buffet
長榮廳 II
Evergreen Room II
長榮廳 I
Evergreen Room I
綠川
River
翠峰
Peak
松濤
Pine
無障礙廁所
Handicapped
Restroom
男廁
Gents'
Restroom
女廁
ladies'
Restroom