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Kyushu Institute of Technology

## WELCOME TO ATS'12

Welcome to the 21st Asian Test Symposium (ATS'12). Since 1992, ATS has been held every year in various Asian cities as the largest symposium that focuses on testing of integrated circuits and systems. Many researchers and engineers from all over the world have attended the past symposia and enjoyed discussions. This year ATS is being held in Niigata as the 7th ATS in Japan.

We have received 99 technical paper submissions from 15 countries and regions, including 47 from Asian countries and regions except Japan, 21 from Europe, 15 from North America and 16 from Japan. Each paper was sent to at least three reviewers for evaluation. The Program Committee meeting was held on July 27, 2012, at Ehime University, and 48 papers were selected based on the reviewers' rating and comments. The selected papers, which cover nearly all aspects of the key area of VLSI testing, were allocated into 15 technical sessions. We have also received six industry paper submissions and all of them are accepted to form an industry session.

In addition to the technical and industry sessions, the ATS program includes two plenary sessions, four two special sessions, one panel session and two half-day tutorials. Two keynote addresses and two invited talks in the plenary sessions are given by Prof. Jacob Abraham, Dr. Shojiro Asai, Prof. Mitsumasa Koyanagi and Dr. Peter Wohl. Four special sessions are organized by Dr. Takahiro Yamaguchi, Prof. Xiaoqing Wen, Prof. Ilia Polian and Dr. Xinli Gu. One panel session is organized also by Dr. Xinli Gu. Two half-day tutorials are offered in cooperation with the Test Technology Test Education Program (TTEP) of IEEE Computer Society, Test Technology Technical Council (TTTC). One is on DFx by Dr. Srikanth Venkataraman and Dr. Robert Aitken and the other is on power-aware testing by Prof. Patrick Girard, Prof. Nicolici and Prof. Xiaoqing Wen.

Finally, we would like to thank the reviewers, the Program Committee members, the Organizing Committee members, and the ATS Steering Committee members for their cooperation. We also thank to all the authors who submitted their works to ATS 2012, and the program participants for their contribution at the symposium.

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Ehime University

Satoshi Ohtake
Program Vice-Chair
Oita University

## Nov. 19, 9:15-12:15, Tutorial 1

**Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliability**

S. Venkataraman (Intel), R. Aitken (ARM)

Summary: The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

## Nov. 19, 13:45-16:45, Tutorial 2

**Power-Aware Testing and Test Strategies for Low Power Devices**

P. Girard (LIRMM),
N. Nicolici (McMaster Univ.),
X. Wen (Kyushu Inst. Tech.)

Summary: Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides

knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability. EDA solutions for considering power during test and design-for-test are also discussed in the last part of the tutorial.

## CALL FOR PARTICIPATION

## The Thirteenth Workshop on RTL and High Level Testing (WRTLT'12)

November 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan

In conjunction with the 21st Asian Test Symposium (ATS'12)

**Nov. 22**
**Registration: 11:30-**
**Opening Session: 13:25-**

**Nov. 23**
**Registration: 8:45-**

**Scopes:**

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. WRTLT'12, the thirteenth workshop, will be held in conjunction with the 21st Asian Test Symposium (ATS'12) in Niigata, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip(SoC) devices and 3D ICs.

## KEYNOTE ADDRESS I

(Nov. 20, 9:50-10:15, Plenary Session 1)

# On-Chip Sensors to Support Parametric Test and Diagnosis

**Jacob A. Abraham**
(University of Texas Austin, Texas, U.S.A.)

Summary: On-chip circuitry, such as a scan chain, has been used for decades to support tests for gate-level faults in digital circuits. However, advances in semiconductor technology down to nano-scale dimensions have enabled the integration of digital, mixed-signal, and RF systems on a single chip. These subsystems need to be tested with limited access from the chip boundary; further, faulty behavior which must be tested includes small delay defects, crosstalk, and voltage droops, as well as deviation from analog and RF specifications. This talk will describe on-chip circuitry for supporting tests for such behavior, including precise measurement of path delays, measuring the skew between specific signals, testing for adherence to analog and RF specifications, detecting substrate noise, and quantifying voltage droops during operation. Simulation and hardware measurement results which demonstrate the necessity and benefits of the DfT techniques will also be presented.

## KEYNOTE ADDRESS II

(Nov. 20, 10:15-10:40, Plenary Session 1)

# VLSI Design and Testing for Enhanced Systems Dependability

**Shojiro Asai**
(CREST DVLSI Program Research Supervisor and
Rigaku Corporation Executive Vice President)

Summary: Very Large-Scale-Integration in monolithic silicon has enabled electronic systems for extensive applications in automobiles, wireless communications, cash/credit/id cards, transportations, power grids, and so force. The reliability inherent and designed in VLSI chips has been a solid foundation for the dependability of such modern-day systems. Threats to the dependability of VLSI actually keep increasing, however, some arising from miniaturization on the one hand and complexity on the other. A research program supported by Japan Science and Technology Agency was started in 2007 to address this challenge and provide basic technologies to enhance dependability at systems as well as VLSI levels. The purpose of this presentation is to give an overall review of the program in an attempt to invite feedback world-wide from outside the program and encourage possible collaborations of mutual interest. It is also intended to provoke a discussion of what appropriate indexes of dependability in VLSI systems are.

## INVITED TALK I

(Nov. 20, 11:00-11:40, Plenary Session 2)

# 3-D Integration Technology and Future Trend

**Mitsumasa Koyanagi**
(New Industry Creation Hatchery Center, Tohoku University)

Summary: 3-D integration technologies are discussed focusing on key technologies such as through-silicon via (TSV), metal microbump, wafer thinning, wafer bonding, wafer alignment and so forth. It is shown that 3-D LSI is suitable for low power operation since the interconnection length can be significantly reduced and the parallel processing can be effectively introduced. In addition, a future new 3-D integration technology and heterogeneous integration technology called a super-chip integration is described. A number of known good dies (KGDs) with different sizes and different devices are simultaneously aligned and bonded onto lower chips or wafer by a chip self-assembly method using the surface tension of liquid in the super-chip integration. Possibilities for new system-on-a chip (SoC) and heterogeneous LSIs by 3-D integration and super-chip integration such as 3-D stacked multicore processor using new shared memory with reconfigurable memory address, 3-D stacked dependable processor with self-test and selfrepair function, GPU stacked 3-D image sensor with extremely fast processing speed, ultra-low power 3-D green LSI with energy scavenger devices operated by reusable energy, 3-D brain-machine interface (BMI) devices etc. are also discussed. Reliability and dependability are significantly important in these new 3-D LSIs. Then influences of 3-D chip stacking and wafer stacking on device characteristic and reliability are discussed referring to mechanical stress and Cu contamination induced by Cu-TSVs andmetal microbumps. It is revealed that device characteristics are deteriorated by mechanical stress induced by TSVs and metal microbumps and Cu contamination. In addition, in order to improve the dependability of 3-D LSIs, it is very important to dynamically test 3-D circuits and self-repair circuit failures using built-in-self-test circuits. It is also important to embed redundancy circuits in 3-D LSIs to replace failure TSVs by good TSVs. Consequently, design for test (DfT) is very important in 3-D LSI design.

## INVITED TALK II

(Nov. 20, 11:40-12:20, Plenary Session 2)

# Next-Generation Testing: Towards a New Level of Abstraction

**Peter Wohl**
(Synopsys, Inc.)

Summary: Electronic systems have arguably sustained the longest and fastest improvement cycle of all human creations. Over a human lifetime, technology, architecture and system integration have yielded orders of magnitude improvement in functionality, performance and price. However, the most enduring advancement is abstraction -- of increasingly higher levels, starting from simple devices and progressing to the complex systems of today and the not yet imagined ones of tomorrow. Testing has evolved alongside these systems and addressed complexity through scan, size through scan compression, power, timing and so on through increasingly sophisticated design-for- (test, manufacturing, diagnosis, etc.) techniques. Adding to the testing challenge, devices and their likely defects are increasingly hard to abstract as statistical process variations lead to blurring the line between “good” and “bad” devices and systems. New testing paradigms have been proposed, such as variation-aware and adaptive testing methods and a variety of integrated on-chip monitors, data processors and controllers. This talk argues that the paradigm shift in the design and test area is evolving into a new level of abstraction that will redefine the roles of design and test engineering, manufacturing and process monitoring. Traditionally, test structures are included in the design; test patterns are generated and then applied on the test floor. Based on data collected during test, the set of applied patterns can somewhat evolve as the process matures and is better understood. This model follows only broad statistical trends and cannot support a new paradigm where each chip can see a different, customized set of test patterns and parameters. At a new level of abstraction, capabilities of testing will be determined by the consumer (the chip) at the time of testing rather than a priori by the producer (the test engineer).

# TUTORIALS

## Nov. 19, 2012

**9:15-12:15 Tutorial 1**
**Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliability**
*S. Venkataraman (Intel), R. Aitken (ARM)*

**13:45-16:45 Tutorial 2**
**Power-Aware Testing and Test Strategies for Low Power Devices**
*P. Girard (LIRMM), N. Nicolici (McMaster Univ.), X. Wen (Kyushu Inst. Tech.)*

# REGULAR SESSIONS

## Nov. 20, 2012

**9:30-10:40 Plenary Session 1**

9:30-9:50 Opening Remarks

9:50-10:15 Keynote Address I:
On-Chip Sensors to Support Parametric Test and Diagnosis
*J. A. Abraham (Univ. Texas)*

10:15-10:40 Keynote Address II:
VLSI Design and Testing for Enhanced Systems Dependability
*S. Asai (CREST and Rigaku Corp.)*

**11:00-12:20 Plenary Session 2**

11:00-11:40 Invited Talk I:
3-D Integration Technology and Future Trend
*M. Koyanagi (Tohoku Univ.)*

11:40-12:20 Invited Talk II:
Next-Generation Testing: Towards a New Level of Abstraction
*P. Wohl (Synopsys)*

**13:40-15:40 Session 3A (Industry Session)**
13:40-14:40 Oral Presentation
14:40-15:40 Poster Presentation

An Effective At-speed Scan Testing Approach Using Multiple-Timing Clock Waveforms
*H. Iwata, Y. Maeda, J. Matsushima, M. Takakura (Renesas)*

LBIST/ATPG Technologies for On-Demand Digital Logic Testing in Automotive Circuits
*D. Meehl, B. Petrakis, P. Zhang (Cadence)*

Portable/Desktop Testing Solution for Engineering with Cloud
*N. Takahashi, T. Watanabe, T. Suzuki, M. Kimura (Advantest)*

Characteristics Variability Evaluation of Actual LSI Transistors with Nanoprobing
*M. Fukui, Y. Nara, J. Fuse (Hitach High-Tech.)*

F-matrix (ABCD-matrix) Circuit Simulation Built in IC Test Program
*H. Okawara (Advantest)*

Addressing Test Challenges in Advanced Technology Nodes
*Y. Zorian (Synopsys)*

**13:40-15:20 Session 3B Diagnosis and Debug**
Chair: *H. -J. Wunderlich (Univ. Stuttgart)*

Diagnosis of Cell Internal Defects With Multi-cycle Test Patterns
*X. Fan (Univ. Iowa), M. Sharama, W. -T. Cheng (Mentor Graphics), S. M. Reddy (Univ. Iowa)*

Automated Post-Silicon Debugging of Failing Speedpaths
*M. Dehbashi (Univ. Bremen), G. Fey (German Aerospace Genter)*

SAT-Based Automatic Rectification and Debugging of Combinational Circuits with LUT Insertions
*S. Jo, T. Matsumoto, M. Fujita (Univ. Tokyo)*

A New Look Ahead Technique for Customized Testing in Digital Microfluidic Biochips
*P. Roy, H. Rahaman (Bengal Engineering and Science Univ.), P. Dasgupta (Indian Inst. Management)*

**13:40-15:20 Session 3C**
**System-in-Package (SiP) / 3D IC Test**
Chair: *D. Xiang (Tsinghua Univ.)*

TSV Stress-Aware ATPG for 3D Stacked ICs
*S. Deutsch, K. Chakrabarty (Duke Univ.), S. Panth, S. K. Lim (Georgia Inst. Tech.)*

Linear Programming Formulations for Thermal-Aware Test-Scheduling of 3D-Stacked Integrated Circuits
*S. K. Millican, K. K. Saluja (Univ. Wisconsin)*

Programmable Leakage Test and Binning for TSVs
*Y. -H. Lin, S. -Y. Huang (National Tsing Hua Univ.), K. -H. Tsai, W. -T. Cheng (Mentor Graphics)*

**ATS Doctoral Thesis Award Contest**
Nov. 20, 14:00-15:20 @Room 303
***Oral Presentation***
Nov. 21, Coffee & Lunch Break @Foyer
***Poster Presentation***

**15:40-17:20 Session 4A (Special Session 1)**
**Quantum Informatics: Classical Circuit Synthesis, Resource Optimisation and Benchmarking**
Organizer: *Ilia Polian (Univ. Passau)*

Counting Gates, Moving Qubits: Evaluating the Execution Cost of Quantum Circuits
*R. V. Meter (Keio Univ.)*

Programming a Topological Quantum Computer
*S. Devitt, K. Nemoto (National Inst. Info.)*

An Optimization Problem for Topological Quantum Computation
*S. Yamashita (Ritsumeikan Univ.)*

Classical Challenge Problems to Realise A Surface Code Quantum Computer
*A. Fowler (Univ. Melbourne)*

**15:40-17:20 Session 4B (Special Session 2)**
**Dependable VLSI**
Organizer: *X. Gu (Huawei Tech.)*

Soft Error Issues with Scaling Technologies
*S. Baeg, J. Bae, S. Lee, C. S. Lim, S. H. Jeon, H. Nam (Hanyang Univ.)*

In-Field Testing of NAND Flash Storage: Why and How?
*Y. Hu (ICT/CAS), X. Gu (Huawei Tech.), X. Li (ICT/CAS)*

A Few Design Techniques for "Dependability" of an SOC
*J. Qian (AMD)*

Accessing Embedded DfT Instruments with IEEE P1687
*E. Larsson (Lund Univ.), F. G. Zadegan (Linkoping Univ.)*

**15:40-17:20 Session 4C Test Compaction / Test Quality**
Chair: *T. Hosokawa (Nihon Univ.)*

Multi-Level EDT to Reduce Scan Channels in SoC Designs
*G. Li, J. Qian, P. Li, G. Zuo (AMD)*

On Utilizing Test Cube Properties to Reduce Test Data Volume Further
*X. Lin, J. Rajski (Mentor Graphics)*

Note on Layout-Aware Weighted Probabilistic Bridge Fault Coverage
*M. Arai, Y. Shimizu, K. Iwasaki (Tokyo Metropolitan Univ.)*

Tailoring Tests for Functional Binning of Integrated Circuits
*S. Sindia, V. D. Agrawal (Auburn Univ.)*

## Nov. 21, 2012

**9:15-10:30 Session 5A Temperature / Power-Aware Test I**
Chair: *M. Yoshimura (Kyushu Univ.)*

A Thermal-Driven Test Application Scheme for 3-Dimensional ICs
*D. Xiang, K. Shen, Y. Deng (Tsinghua Univ.)*

A Transition Isolation Scan Cell Design for Low Shift and Capture Power
*Y. -T. Lin, J. -L. Huang (National Taiwan Univ.), X. Wen (Kyushu Insti. Tech.)*

A Probabilistic and Constraint Based Approach for Low Power Test Generation
*H. Sabaghian-Bidgoli, M. Namaki-Shoushtari, Z. Navabi (Univ. Tehran)*

**9:15-10:30 Session 5B**
**Dependable Systems / Memory Test**
Chair: *S.Gupta (Univ. Southern California)*

Dual Edge Triggered Flip-Flops for Noise Blocking and Application to Signal Delay Detection
*Y. Ohkawa, Y. Miura (Tokyo Metropolitan Univ.)*

Impact of Resistive-Bridge Defects in TAS-MRAM Architectures
*J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri (LIRMM), G. Prenat (CEA/SPINTEC), J. Alvarez-Herault, K. Mackay (CROCUS Tech.)*

SoftPCM: Enhancing Energy Efficiency and Lifetime of Phase Change Memory in Video Applications via Approximate Write
*Y. Fang, H. Li, X. Li (ICT/CAS)*

**9:15-10:30 Session 5C**
**Design Verification and Validation / Software Design for Testing**
Chair: *S. Fukumoto (Tokyo Metropolitan Univ.)*

A Generalized Theory for Formal Assertion Coverage
S. Das (IIT Kharagpur), A. Banerjee (Indian Statistical Inst.), *P. Dasgupta (IIT Kharagpur)*

Error Model Free Automatic Design Error Correction of Complex Processors Using Formal Methods
*A. M. Gharehbaghi (JST), M. Fujita (Univ. Tokyo)*

Hardware-Accelerated Workload Characterization for Power Modeling and Fault Injection
*A. Krieg, J. Grinschgl, C. Steger, R. Weiss (Graz Univ.), H. Bock, J. Haid (Infineon Tech.),*

**ATS Doctoral Thesis Award Contest**
Nov. 20, 14:00-15:20 @Room 303
***Oral Presentation***
Nov. 21, Coffee & Lunch Break @Foyer
***Poster Presentation***

**10:50-12:30 Session 6A**
**Temperature / Power-Aware Test II**
Chair: *H. Li (ICT/CAS)*

Scan Test Power Simulation on GPGPUs
*S. Holst, E. Schneider, H. -J. Wunderlich (Univ. Stuttgart)*

Power Supply Noise Sensor based on Timing Uncertainty Measurements
*M. Valka, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM), P. Debaud, S. Guilhot (ST-Ericsson)*

Peak Power Estimation: a Case Study on CPU Cores
*P. Bernardi, M. D. Carvalho, E. Sanchez, M. S. Reorda (Politecnico di Torino), A. Bosio, L. Dilillo, P. Girard, M. Valka (LIRMM)*

Low Power BIST for Scan-Shift and Capture Power
*Y. Sato, S. Wang, T. Kato, K. Miyase, S. Kajihara (Kyushu Inst. Tech.)*

**10:50-12:30 Session 6B**
**Analog Test and High-Speed I/O Test I**
Chair: *M. Hashizume (Univ. Tokushima)*

Two-Tone Signal Generation for Communication Application ADC Testing
*K. Kato, F. Abe, K. Wakabayashi, C. Gao, T. Yamada, H. Kobayashi (Gunma Univ.), O. Kobayashi (STARC), K. Niitsu (Gunma Univ.)*

A New Procedure for Measuring High-Accuracy Probability Density Functions
*T. J. Yamaguchi (Advantest), K. Asada (Univ. Tokyo), K. Niitsu (Gunma Univ.), M. Abbas, S. Komatsu (Univ. Tokyo), H. Kobayashi (Gunma Univ.), J. A. Moreira (Advantest)*

Design of a High Bandwidth Interposer for Performance Evaluation of ATE Test Fixtures at the DUT Socket
*J. Moreira (Advantest)*

Spectral Estimation Based Acquisition of Incoherently Under-sampled Periodic Signals : Application to Bandwidth Interleaving
*D. Bhatta, N. Tzou (Georgia Inst. Tech.), H. Choi (Samsung), A. Chatterjee (Georgia Inst. Tech.)*

**10:50-12:30 Session 6C Board and System Test**
Chair: *K. -J. Lee (National Cheng Kung Univ.)*

Adaptive Board-Level Functional Fault Diagnosis Using Decision Trees
*F. Ye (Duke Univ.), Z. Zhang (Huawei Tech.), K. Chakrabarty (Duke Univ.), X. Gu (Huawei Tech.)*

Board-Level Functional Fault Diagnosis Using Learning Based on Incremental Support-Vector Machines
*F. Ye (Duke Univ.), Z. Zhang (Huawei Tech.), K. Chakrabarty (Duke Univ.), X. Gu (Huawei Tech.)*

Reuse of Structural Volume Test Methods for In-System Testing of Automotive ASICs
*A. Cook, D. Ull, M. Elm, H. -J. Wunderlich (Univ. Stuttgart), H. Randoll, S. Döhren (Bosch)*

**13:30-15:10 Section 7A (Special Session 3)**
**Power-Aware Testing: Present and Future**
Organizer: *X. Wen (Kyushu Inst. Tech.)*
Moderator: *S.M. Reddy (Univ. Iowa)*

Why and How Controlling Power Consumption During Test: A Survey
*A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM)*

PowerMAX: Fast Power Analysis during Test
*W. Zhao, M. Tehranipoor (Univ. Connecticut)*

Current and Future Directions in Automatic Test Pattern Generation for Power Delivery Network Validation
*P. Varma (Apache Design)*

Power-Supply Droop and Its Impacts on Structural At-Speed Testing
*X. Lin (Mentor Graphics)*

**13:30-15:10 Section 7B**
**Special Session 4: Post-Silicon Measurements and Tests**
**Regular Session: Analog Test and High Speed I/O Test II**
Organizer: *T. J. Yamaguchi (Advantest)*

**(Special Session)**
A Test Screening Method for 28nm HK/MG Single-Port and Dual-Port SRAMs Considering with Dynamic Stability and Read/Write Disturb Issues
*K. Nii, Y. Tsukamoto, Y. Ishii, M. Yabuuchi, H. Fujiwara, K. Okamoto (Renesas)*

Impact of All-Digital PLL on SoC Testing
*T. Nakura, T. Iizuka, K. Asada (Univ. Tokyo)*

**(Regular Session)**
Post-Silicon Jitter Measurements
*K. Niitsu (Gunma Univ.), T. J. Yamaguchi, M. Ishida (Advantest), H. Kobayashi (Gunma Univ.)*

An Active Test Fixture Approach for Testing 28 Gbps Applications Using a Lower Data Rate ATE System
*J. Moreira, B. Roth, C. McCowan (Advantest)*

**13:30-15:10 Section 7C Panel: Board / System Test**

Is Componet Interconnection Test Enough for Board or System Test?

Panel Moderator: *X. Gu, (Huawei Tech.)*

Panelists:

*X. Gu, (Huawei Tech.)*
*S. Kameyama, (Fujitsu)*
*M. Keim, (Mentor Graphics)*
*J. Qian, (AMD)*
*K. Chakrabarty, (Duke Univ.)*

***15:20- Social Program***

**Nov. 22, 2012**

**9:15-10:30 Session 8A**
**Embedded Tutorial: Yield Analysis Diagnosis for Accelerating Yield and Failure**

Chair: *K. S. -M. Li (National Sun Yat-sen Univ.)*

*W. -T. Cheng (Mentor Graphics),*
*F. -M. Kuo (TSMC)*

**9:15-10:30 Session 8B Built-In Test and Built-In Characterization Technique**

Chair: *X. Li (ICT/CAS)*

A Scan-Out Power Reduction Method for Multi-Cycle BIST
*S. Wang, Y. Sato, K. Miyase, S. Kajihara (Kyushu Inst. Tech.)*

A Test-Per-Clock LFSR Reseeding Algorithm for Concurrent Reduction on Test Sequence Length and Test Data Volume
*W. -C. Lien, K. -J. Lee (National Cheng Kung Univ.), T. -Y. Hsieh (National Sun Yat-sen Univ.)*

A Built-In Characterization Technique for 1-Bit/Stage Pipelined ADC
*Y.-H. Chou, J. -L. Huang, X. -L. Huang (National Taiwan Univ.)*

**9:15-10:30 Session 8C ATPG**
Chair: *Y. Higami (Ehime Univ.)*

Robust Timing-Aware Test Generation Using Pseudo-Boolean Optimization
*S. Eggersglüß (Univ. Bremen), M. Yilmaz (NVIDIA), K. Chakrabarty (Duke Univ.)*

Functional Pattern Generation for Asynchronous Designs in a Test Processor Environment
*S. Zeidler, C. Wolf, M. Krstić, R. Kraemer (IHP)*

Reduced-Complexity Transition-Fault Test Generation for Non-Scan Circuits through High-Level Mutant Injection
*V. Guarnieri, F. Fummi (Univ. Verona), K. Chakrabarty (Duke Univ.)*

**10:50-12:05 Session 9A Yield Analysis and Enhancement**
Chair: *S. -Y. Huang (National Tsing Hua Univ.)*

Scrambling and Data Inversion Techniques for Yield Enhancement of NROM-Based ROMs
*S. -K. Lu, T. -L. Li (National Taiwan Univ.), P. Ning (Nanya Tech.)*

A Hybrid Flow for Memory Failure Bitmap Classification
*J. Li (Tsinghua Univ.), Y. Huang, W. -T. Cheng, C. Schuermyer (Mentor Graphics), D. Xiang (Tsinghua Univ.), E. Faehn (STMicroelectronics), R. Farrugia (STEricsson)*

Test Cost Reduction for Performance Yield Recovery by Classification of Multiple-Clock Test Data
*J. -H. Kuo, T. -S. Hsu, J. -J. Liou (National Tsing Hua Univ.)*

**10:50-12:05 Session 9B DFT / On-Line Test**
Chair: *P. Bernardi (Politecnico di Torino)*

NoC Dynamically Reconfigurable as TAM
*T. Sbiai, K. Namba (Chiba Univ.)*

On-Line Error Detection in Digital Microfluidic Biochips
*D. Mitra (National Institute of Technology), S. Ghoshal, H. Rahaman (Bengal Engineering & Science Univ.), K. Chakrabarty (Duke Univ.), B. B. Bhattacharya (Indian Statistical Inst.)*

Automatic Test Program Generation for Out-of-Order Superscalar Processors
*Y. Zhang, A. Rezine, P. Eles, Z. Peng (Linkoping Univ.)*

**10:50-12:05 Session 9C Delay and Performance Test**
Chair: *Y. Sato (Kyushu Inst. Tech.)*

Variation-Aware Fault Grading
*A. Czutro (Univ. Freiburg), M. E. Imhot (Univ. Stuttgart), J. Jiang (Univ. Passau), A. Mumtaz (Univ. Stuttgart), M. Sauer, B. Becker (Univ. Freiburg), I. Polian (Univ. Passau), H. -J. Wunderlich (Univ. Stuttgart)*

On-Chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation
*I. A. K. M. Mahfuzul, H. Onodera (Kyoto Univ.)*

Efficient Trojan Detection via Calibration of Process Variations
*B. Cha, S. K. Gupta (Univ. Southern California)*

## REGISTRATION DESK

The registration desk will be found at foyer of the 3rd floor in the convention center (Toki Messe). It will be open during the following hours:

Nov. 19, Mon. 8:45-20:00
Nov. 20, Tue. 8:45-17:00
Nov. 21, Wed. 8:45-15:30

## SOCIAL EVENTS

***Welcome Reception:***

The welcome reception will be held in ***Room Toki***, on the ***4th floor*** of ***Hotel Nikko Niigata*** on ***Monday, Nov. 19, from 18:00***. The hotel is located next to the conference site (Toki Messe). Light meals, snacks and drinks will be provided.

***Tour and Banquet:***

The conference registration fee for Member and Non-member includes a local tour and a conference banquet on Nov. 21, from 15:20. You will find a banquet ticket in your name holder. The tour takes you to the Northern Culture Museum by bus. The museum was the house of large landowner. It has traditional Japanese architectures and a beautiful garden. After visiting the museum, we will enjoy a banquet at the Garden House Ikarashi. The banquet will begin with Sake Barrel Opening Ceremony and include attractive events.

## WIRELESS ACCESS

Wireless access to the internet will be available to participants. Information for connecting to the network will be available at the registration desk.

## PROGRAM COMMITTEE

Takashi Aikyo
Kenichi Anzo
Davide Appello
Karim Arabi
Krishnendu Chakrabarty
Chia-Tso Chao
Vivek Chickermane
Debesh Kumar Das
Serge Demidenko
Jennifer Dworak
Stefan Eichenberger
Patrick Girard
Dimitris Gizopoulos
Xinli Gu
Said Hamdioui
Kiyoharu Hamaguchi
Masaki Hashizume
Yoshinobu Higami
Michael S. Hsiao
Yu Huang
Michiko Inoue
Sungho Kang
Haruo Kobayashi
Erik Larsson
Kuen-Jong Lee
Huawei Li
Erik Jan Marinissen
Teresa McLaurin
Cecilia Metra
Fidel Muradali
Koji Nakamae
Yoshiyuki Nakamura
Michinobu Nakao
Hiroyuki Nakamura
Kazuteru Namba
Kenzo Okumura
Chia Yee Ooi
Alex Orailoglu
Adam Osseiran
Sule Ozev
Sungju Park
Irith Pomeranz
Rajesh Raina
Srivaths Ravi
Antonio Rubio
Masaru Sanada
Yasuo Sato
Arani Sinha
Virendra Singh
Peilin Song
Chau-Chin Su
Mohammad Tehranipoor
Tatsuhiro Tsuchiya
Srikanth Venkataraman
Andreas Veneris
Sying-Jyan Wang
Li-C. Wang
Xiaoqing Wen
Peter Wohl
Cheng-Wen Wu
Hans-Joachim Wunderlich
Dong Xiang
Qiang Xu
Shiyi Xu
Takahiro Yamaguchi
Masayoshi Yoshimura
Danella Zhao