Information

Latest News!!

Online Registration has been closed!

Sponsored by
IEEE Computer Society Test Technology Technical Council
Kyushu Institute of Technology

In cooperation with
The IEICE Information and Systems Society Technical Committee on Dependable Computing
Japan Science and Technology Agency

Scopes
The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all
countries of the world, especially from Asia, to present and discuss various aspects of device, board and
system testing with design, manufacturing and field considerations in mind.

Major topics include, but are not limited to:

- Automatic Test Pattern Generation (ATPG)
- Analog Test / Mixed-Signal Test
- Boundary Scan Test
- Board and System Test
- Built-In Self-Test
- Design for Testability (DFT)
- Design Verification and Validation
- Defect-Based Testing
- Delay and Performance Test
- Fault Modeling and Simulation
- Fault Tolerance
- High-Speed I/O Test / RF Testing
- Memory Test / FPGA Test
- On-Line Test
- System-on-a-Chip Test
- System-in-package (SiP)/ 3D Test
- Software Testing / Software Design for Testing
Submissions

Regular Session:
The ATS'12 Program Committee invites original, unpublished paper submissions for ATS'12. Paper submissions should be complete manuscripts, up to six pages (including figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. (For more details...)

Key Dates (Regular Session)
Camera ready copy: Aug. 31, 2012

Industry Session:
This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. (For more details...)

Key Dates (Industry Session)
Notification of acceptance: Aug. 5, 2012
Camera ready copy: Aug. 31, 2012

Doctoral Thesis Award:
The Award serves the purpose to promote most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology. This major Award is named after Prof. Edward J. McCluskey, a key educator and mentor in the fields of test technology, logic design, and reliability. CFP(pdf)

Key Dates (Doctoral Thesis Award)
Submission deadline: Sep. 5th, 2012
Notification of acceptance: Sep. 20, 2012

More Information

For general information
General Chair: Kazumi Hatayama (ats12-gc@aries30.cse.kyutech.ac.jp)

For submission related information
Program Chair: Hiroshi Takahashi (ats12-pc@aries30.cse.kyutech.ac.jp)
The 21st Asian Test Symposium  
November 19-22, 2012, Toki Messe Niigata Convention Center, Niigata, Japan

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### Registration Fee

<table>
<thead>
<tr>
<th>Category</th>
<th>Early Registration (on and before October 18, 2012)</th>
<th>Late Registration (on and after October 19, 2012)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symposium (Members)</td>
<td>JPY 45,000</td>
<td>JPY 54,000</td>
</tr>
<tr>
<td>Symposium (Non-members)</td>
<td>JPY 57,000</td>
<td>JPY 69,000</td>
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<tr>
<td>Symposium (Student/Life/Retired members)</td>
<td>JPY 11,000</td>
<td>JPY 13,000</td>
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<tr>
<td>Symposium (Student non-members)</td>
<td>JPY 14,000</td>
<td>JPY 17,000</td>
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<tr>
<td>Symposium 1st-day-only [Nov.20] (Members)</td>
<td>JPY 27,000</td>
<td>JPY 27,000</td>
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<tr>
<td>Symposium 1st-day-only [Nov.20] (Non-members)</td>
<td>JPY 34,000</td>
<td>JPY 34,000</td>
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<tr>
<td>Tutorial Full Day (Members)</td>
<td>JPY 23,000</td>
<td>JPY 30,000</td>
</tr>
<tr>
<td>Tutorial Full Day (Non-members)</td>
<td>JPY 32,000</td>
<td>JPY 42,000</td>
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<tr>
<td>Tutorial Full Day Others (Student/Life/Retired)</td>
<td>JPY 13,000</td>
<td>JPY 17,000</td>
</tr>
<tr>
<td>Tutorial Half Day (Members)</td>
<td>JPY 14,000</td>
<td>JPY 18,000</td>
</tr>
<tr>
<td>Tutorial Half Day (Non-members)</td>
<td>JPY 18,000</td>
<td>JPY 25,000</td>
</tr>
<tr>
<td>Tutorial Half Day Others (Students/Life/Retired)</td>
<td>JPY 9,000</td>
<td>JPY 11,000</td>
</tr>
</tbody>
</table>

*Extra social event tickets  JPY10,000

**Registration fee includes:**
- Proceedings
- Social event (reception on Nov.19, tour, banquet on Nov.21)

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*IEEE member rate is also applied for IEICE members.
*Registration fee for IEEE member and Non-member includes social event tickets.
*Student/Life/Retired member fees do not include the social event (the reception, the tour and the banquet).
*At least one author must register with the paper reference number by September 7.
*Participant lists including name, affiliation, and country will be distributed to attendees.
*If you need to cancel or edit, please contact westec_op13@west.jtb.jp
*If you need change of item about receipt, Please contact westec_op13@west.jtb.jp
*We will pass invoice at the venue on the day.

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**For domestic participants:**
日本の方はお支払いの際、銀行振込にてお願いいたします。
会議の運営経費削減にご協力ください。

---

### Registration Procedure

Please complete your registration by logging-in to your “My Page”.
If you have not yet registered your personal information, please first complete the required items on the ID Application page in order to obtain a log-in ID and Password.

### Payment Procedure

After you complete your reservation, please click the “Full Payment” button displayed on the Payment Status page.
Credit Card payment, Convenience Store payment, Pay-easy are acceptable for the Symposium. In order to make your reservation, a full deposit will be necessary. Payment must be made latest on or before 5 November, 2012.

[How to pay by credit card]
The credit cards listed below can be used to make payments.

*Visa, MasterCard®, JCB, AMEX, Dinners Club*
1. For VISA, Master Card®, and JCB cardholders

This system supports 3-D Secure for certain cardholders in order to provide a more secure online payment experience.

What is 3-D Secure?

This system adds an authentication step to the online payment process by requiring the user to enter a previously registered password on an authentication screen provided by the credit card issuer. International credit card brands VISA, MasterCard®, and JCB recommend that merchants make use of this system.

Credit card issuers use different names to refer to their implementation of 3-D Secure, including Verified by VISA (used by VISA), MasterCard® SecureCode™ (MasterCard®), and J/Secure™ (JCB).

*Some issuers allow cardholders to use the same password they have been assigned for accessing their monthly statements online or having them sent by email. If this password is not entered, or if an incorrect password is entered, the online transaction will not be completed.

*If you forget your password or experience other authentication-related issues, please contact your credit card issuer. (For more information, see your credit card issuer’s website.)

*In terms of the actual payment process, once you have entered your card information (issuer, card number, expiration date, and cardholder name), click the “Next” button to proceed to the credit card issuer’s authentication screen.

2. For AMERICAN EXPRESS (AMEX) and Diners Club International cardholders

Card number, expiration date and security code will be required for the payment.

*The security code is the last 3 digits of the number printed above the card holder signature area on the back of the card.

*For American Express cards, this is the 4 digits number stamped above the card number on the front of the card.

For more details on the credit card payment, please refer to *About Payment* on My Page.

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日本の方はお支払いの際、銀行振込にて御願いいたします。
会議の運営経費削減にご協力ください。

*銀行振込での手順が不明な場合は、JTBまでご連絡をお願い致します。（westec_op13@west.jtb.jp）
  お振込先情報をお送りさせていただきます。
*銀行振込の際の振込手数料はご参加者様負担となりますので、お知らせ承りお願いいたします。
*銀行振込の際の振込金額の上限は、10月25日までです。参加登録後、1週間以内にお振込お願い致します。
*Early Registration期間中にお振込が確認できない場合は、Late Registrationの料金が適用されますので、ご注意ください。
*WEB上での事前受付の終了後は、当日現金にてお支払いただきます。

Confirmation

Your registration will be completed upon receipt of your online registration information and payment. A "Confirmation sheet" button will be displayed when you complete your registration. Please print out your confirmation slip by clicking the "Confirmation sheet" button and bring it with you to the On-site Registration Desk.

Cancellation

*In case of cancellation, your registration fee will be refunded after deducting the cancellation fees as shown below.
*Please note all refunds will be made after the end of the Conference/the Symposium.

<table>
<thead>
<tr>
<th>Cancellation Fee</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>On or Before October 18</td>
<td>JPY 5,000</td>
</tr>
<tr>
<td>On or After October 19</td>
<td>100% of the registration fee/No refund</td>
</tr>
</tbody>
</table>

If you wish to cancel your registration, please contact westec_op13@west.jtb.jp.

Deadline for Registration

The deadline for online registration is 23:59 of November 5, 2012, Japan Standard Time (GMT+9)

Inquiries for Registration

Please send us your inquiries by logging-in to your "My Page" and clicking on the "Inquiry" button.

JTB Western Japan Corp.,
MICE Center
IEEE Asian Test Symposium 2012

TEL: +81-6-6252-2861
FAX: +81-6-6252-2862
E-mail: westec_op13@west.jtb.jp
Office hours: 9:30-17:30 (weekdays only)
## Accommodations Application Procedures

### General Information
JTB Western Japan Corp. (JTB) has been appointed as an official travel agent for the Conference and will handle hotel accommodations.

- Hotel assignment will be made on a first-come, first-served basis.
- Please check the hotel list for details of accommodations.
- Rates are valid for the stay from November 18, 19, 20, 21, 22, to 23, 2012.
- The hotel rates are per person, per night, including service charge and consumption tax with Breakfast.
- All guests are required to make own arrangements to the hotel from airports or railway stations.
- Minimum number required is 1 person.

### Hotel Information
*Please click on each hotel name to confirm hotel information.
*You can check hotel fees of each day or room type by clicking on “Room Rate”.

<table>
<thead>
<tr>
<th>Hotel Name</th>
<th>Room Type</th>
<th>Room Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Hotel Nikko Niigata</td>
<td>Single room 1 person(s) with breakfast</td>
<td>JPY10,500 Room Rate</td>
</tr>
<tr>
<td></td>
<td>Twin room 1 person(s) to 2 person(s) with breakfast</td>
<td>JPY9,500 to JPY15,500 Room Rate</td>
</tr>
<tr>
<td>2. ANA Crowne Plaza Hotel Niigata</td>
<td>Single room 1 person(s) with breakfast</td>
<td>JPY12,050 Room Rate</td>
</tr>
<tr>
<td></td>
<td>Twin room 1 person(s) to 2 person(s) with breakfast</td>
<td>JPY9,975 to JPY14,700 Room Rate</td>
</tr>
<tr>
<td>3. Niigata Tokyu Inn</td>
<td>Single room 1 person(s) with breakfast</td>
<td>JPY7,900 Room Rate</td>
</tr>
<tr>
<td></td>
<td>Twin room 1 person(s) to 2 person(s) with breakfast</td>
<td>JPY6,900 to JPY10,400 Room Rate</td>
</tr>
<tr>
<td>4. Niigata Daichi Hotel</td>
<td>Single room 1 person(s) with breakfast</td>
<td>JPY8,850 Room Rate</td>
</tr>
<tr>
<td></td>
<td>Twin room 1 person(s) to 2 person(s) with breakfast</td>
<td>JPY6,450 to JPY9,050 Room Rate</td>
</tr>
<tr>
<td>5. Niigata Station Hotel</td>
<td>Single room 1 person(s) with breakfast</td>
<td>JPY6,800 Room Rate</td>
</tr>
<tr>
<td></td>
<td>Twin room 1 person(s) to 2 person(s) with breakfast</td>
<td>JPY6,275 to JPY7,850 Room Rate</td>
</tr>
</tbody>
</table>

### Reservation Procedure
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For more details on the credit card payment please refer to *About Payment* on My Page.

*If you would like to pay by bank transfer, please contact westec_op13@west.itb.jp
*In case of bank transfer, a remittance fee will be added to your remittance form.
*If you need change of item about receipt, Please contact westec_op13@west.itb.jp

Confirmation
The Confirmation button will be displayed when you complete your reservation. Please print your confirmation slip by clicking the Confirmation button and bring it with you to the reception desk upon checking-in at the hotel.

Cancellation / Revision
*In case of cancellation, your deposit will be refunded after deducting the cancellation fees as follows.
*Please revise and/or cancel your reservation by logging-in to your "My Page".
*Cancellation fee when notice is given

8 days or more days prior to the first night of stay...0% of daily room rate
2 to 7 days before the first night of stay...20% of daily room rate
1 day before the first night of stay...40% of daily room rate
The first night of stay if notice given before noon(Japan Time) on check-in day...50% of daily room rate
The first night of stay if no notice given...100% of daily room rate

Deadline for Accommodations
The deadline for Reservations on this site is 23:59 of November 5, 2012 Japan Standard Time (GMT+9)
(Please note that reservations will also be closed when all the accommodations have become full.)

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ATS'12 at a Glance

<table>
<thead>
<tr>
<th>Nov.19 (Mon.)</th>
<th>Room 302 A/B</th>
<th>Room 301 A</th>
<th>Room 301 B</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:15-12:15</td>
<td></td>
<td></td>
<td>Tutorial 1 (Room 301 B)</td>
</tr>
<tr>
<td>12:15-13:45</td>
<td></td>
<td></td>
<td>Lunch Time</td>
</tr>
<tr>
<td>13:45-16:45</td>
<td></td>
<td></td>
<td>Tutorial 2 (Room 301 B)</td>
</tr>
<tr>
<td>18:00-</td>
<td></td>
<td></td>
<td>Welcome Reception (Hotel Nikko Niigata 4F)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Nov.20 (Tue.)</th>
<th>Room 302 A/B</th>
<th>Room 301 A</th>
<th>Room 301 B</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:30-10:40</td>
<td></td>
<td></td>
<td>Plenary Session 1 (Marine Hall)</td>
</tr>
<tr>
<td>10:40-11:00</td>
<td></td>
<td></td>
<td>Coffee Break</td>
</tr>
<tr>
<td>11:00-12:20</td>
<td></td>
<td></td>
<td>Plenary Session 2 (Marine Hall)</td>
</tr>
<tr>
<td>12:20-13:40</td>
<td></td>
<td></td>
<td>Lunch Time</td>
</tr>
<tr>
<td>13:40-15:20</td>
<td>3A Industry Session</td>
<td>3B Diagnosis and Debug</td>
<td>3C System-in-Package (SiP)/3D IC Test</td>
</tr>
<tr>
<td>13:40-14:40</td>
<td>Oral @ 302A/B</td>
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<td>Poster @ Foyer</td>
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<tr>
<td>14:40-15:40</td>
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<td></td>
<td>3B Dependable VLSI Dependable Systems/Memory Test</td>
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<tr>
<td>15:20-15:40</td>
<td></td>
<td></td>
<td>4C Test Compaction/Test Quality</td>
</tr>
<tr>
<td>15:40-17:20</td>
<td>4A (Special Session 1) Quantum Informatics</td>
<td>5B (Special Session 2) Dependable VLSI Dependable Systems/Memory Test</td>
<td>5C Design Verification and Validation/Software Design for Testing</td>
</tr>
<tr>
<td>9:15-10:30</td>
<td>5A Temperature / Power-Aware Test I</td>
<td>5B Dependable Systems/Memory Test</td>
<td>5C Design Verification and Validation/Software Design for Testing</td>
</tr>
<tr>
<td>10:30-10:50</td>
<td></td>
<td></td>
<td>Coffee Break</td>
</tr>
<tr>
<td>10:50-12:30</td>
<td>6A Temperature / Power-Aware Test II</td>
<td>6B Analog Test and High-Speed 1/O Test I</td>
<td>6C Board and System Test</td>
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<tr>
<td>Nov. 21 (Wed.)</td>
<td>Nov. 22 (Thu)</td>
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<tr>
<td>12:30-13:30</td>
<td>Lunch Time</td>
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<tr>
<td>13:30-15:10</td>
<td>7A (Special Session 3) Power-Aware Testing: Present and Future</td>
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<tr>
<td></td>
<td>7B (Special Session 4) Post-Silicon Measurements and Tests (Analogue Test and High-Speed I/O Test II)</td>
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<td></td>
<td>7C Panel: Board / System Test</td>
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<tr>
<td>15:20-22:00</td>
<td>Social Program</td>
<td></td>
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<tr>
<td>9:15-10:30</td>
<td>8A Embedded Tutorial Yield Analysis</td>
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<td></td>
<td>8B Built-In Test and Built-In Characterization Technique</td>
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<td></td>
<td>8C ATPG</td>
<td></td>
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<tr>
<td>10:30-10:50</td>
<td>Coffee Break</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:50-12:05</td>
<td>9A Yield Analysis and Enhancement</td>
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<td></td>
<td>9B FDT/On-Line Test</td>
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<tr>
<td></td>
<td>9C Delay and Performance Test</td>
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</tr>
</tbody>
</table>
ATS'12 Advance Program

Jump to November 19th, 20th, 21st, 22nd

Nov. 19th, 2012

9:15-12:15 Tutorial 1
Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliability
S. Venkataraman (Intel), R. Aitken (ARM)

13:45-16:45 Tutorial 2
Power-Aware Testing and Test Strategies for Low Power Devices
P. Girard (LIRMM), N. Nicolici (McMaster Univ.), X. Wen (Kyushu Inst. Tech.)

Nov. 20th, 2012

9:30-10:40 Plenary Session 1
Keynote Address I:
On-Chip Sensors to Support Parametric Test and Diagnosis
J. A. Abraham (Univ. Texas)

Keynote Address II:
VLSI Design and Testing for Enhanced Systems Dependability
S. Asai (CREST and Rigaku Corp.)

11:00-12:20 Plenary Session 2
Invited Talk I:
3-D Integration Technology and Future Trend
M. Koyanagi (Tohoku Univ.)

Invited Talk II:
Next-Generation Testing: Towards a New Level of Abstraction
P. Wohl (Synopsys)

13:40-15:40 Session 3A (Industry Session)
13:40-14:40 Oral Presentation
14:40-15:40 Poster Presentation
An Effective At-speed Scan Testing Approach Using Multiple-Timing Clock Waveforms
H. Iwata, Y. Maeda, J. Matsushima, M. Takakura (Renesas)

LBIST/ATPG technologies used for on-demand digital logic testing in Automotive Circuits
D. Meehl, B. Petrakis, P. Zhang (Cadence)
Portable/Desktop Testing Solution for Engineering with Cloud
N. Takahashi, T. Watanabe, T. Suzuki, M. Kimura (Advantest)
Characteristics Variability Evaluation of Actual LSI Transistors with Nanoprobing
M. Fukui, Y. Nara, J. Fuse (Hitach High-Tech.)
F-matrix (ABCD-matrix) Circuit Simulation Built in IC Test Program
H. Okawara (Advantest)
Addressing Test Challenges in Advanced Technology Nodes
Y. Zorian (Synopsys)

13:40-15:20 Session 3B Diagnosis and Debug
Chair: H. -J Wunderlich (Univ. Stuttgart)
Diagnosis of Cell Internal Defects With Multi-Cycle Test Patterns
X. Fan (Univ. Iowa), M. Sharama, W. -T. Cheng ( Mentor Graphics), S. M. Reddy (Univ. Iowa)
Automated Post-Silicon Debugging of Failing Speedpaths
M. Dehbash (Univ. Bremen), G. Fey (German Aerospace Center)
SAT-based automatic rectification and debugging of combinational circuits with LUT insertions
S. Jo, T. Matsumoto, M. Fujita (Univ. Tokyo)
A new look ahead technique for customized testing in Digital Microfluidic Biochips
P. Roy, H. Rahaman (Bengal Engineering and Science Univ.), P. Dasgupta (Indian Inst. Management)

13:40-15:20 Session 3C System-in-Package (SiP) / 3D IC Test
Chair: D. Xiang (Tsinghua Univ.)
TSV Stress-Aware ATPG for 3D Stacked ICs
S. Deutsch, K. Chakrabarty (Duke Univ.), S. Panth, S. K. Lim (Georgia Inst. Tech.)
Linear Programming Formulations for Thermal-Aware Test-Scheduling of 3D-Stacked Integrated Circuits
S. K. Millican, K. K. Saluja (Univ. Wisconsin)
Programmable Leakage Test and Binning for TSVs

15:40-17:20 Session 4A (Special Session 1)
Quantum Informatics: Classical Circuit Synthesis, Resource Optimisation and Benchmarking
Organizer: Ilia Polian (Univ. Passau)
Counting Gates, Moving Qubits: Evaluating the Execution Cost of Quantum Circuits
R. V. Meter (Kyoto Univ.)
Programming a Topological Quantum Computer
S. Devitt, K. Nemoto (National Inst. Info.)
An Optimization Problem for Topological Quantum Computation
S. Yamashita (Ritsumeikan Univ.)
Classical challenge problems to realise a surface code quantum computer
A. Fowler (Univ. Melbourne)

15:40-17:20 Session 4B (Special Session 2)
Dependable VLSI
Organizer: X. Gu (Huawei Tech.)
Soft Error Issues with Scaling Technologies
S. Baeg, J. Bae, S. Lee, C. S. Lim, S. H. Jeon, H. Lee (Hanyang Univ.)
In-field Testing of NAND Flash Storage: Why and How?
Y. Hu (ICT/CAS), X. Gu (Huawei Tech.), X. Li (ICT/CAS)
A Few Design Techniques for "Dependability" of an SOC
J. Qian (AMD)
Accessing Embedded DfT Instruments with IEEE P1687

15:40-17:20 Session 4C Test Compaction / Test Quality
Chair: T. Hosokawa (Nihon Univ.)
Multi-Level EDT to Reduce Scan Channels in SoC Designs
G. Li, J. Qian, P. Li, G. Zuo (AMD)
On Utilizing Test Cube Properties to Reduce Test Data Volume Further
X. Lin, J. Rajski (Mentor Graphics)
Note on Layout-Aware Weighted Probabilistic Bridge Fault Coverage
M. Arai, Y. Shimizu, K. Iwasaki (Tokyo Metropolitan Univ.)
Tailoring Tests for Functional Binning of Integrated Circuits
S. Sindia, V. D. Agrawal (Auburn Univ.)

Nov. 21st, 2012
9:15-10:30 Session 5A Temperature / Power-Aware Test I
Chair: M. Yoshimura (Kyushu Univ.)
A Thermal-Driven Test Application Scheme for 3-Dimensional ICs
D. Xiang, K. Shen, Y. Deng (Tsinghua Univ.)
A Transition Isolation Scan Cell Design for Low Shift and Capture Power
Y. -T. Lin, J. -L. Huang (National Taiwan Univ.), X. Wen (Kyushu Insti. Tech.)
A Probabilistic and Constraint Based Approach for Low Power Test Generation
H. Sabaghian-Bidgoli, M. Namaki-Shoushtari, Z. Navabi (Univ. Tehran)

9:15-10:30 Session 5B Dependable Systems / Memory Test
Chair: S. Gupta (Univ. Southern California)
Dual Edge Triggered Flip-Flops for Noise Blocking and Application to Signal Delay Detection
Y. Ohkawa, Y. Miura (Tokyo Metropolitan Univ.)
Impact of Resistive-Bridge Defects in TAS-MRAM Architectures
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri (LIRMM), G. Prenat
CEA/SPINTEC), J. Alvarez-Herault, K. Mackay (CROCUS Tech.)
SoftPCM: Enhancing Energy Efficiency and Lifetime of Phase Change Memory in Video
Applications via Approximate Write
Y. Fang, H. Li, X. Li (ICT/CAS)

9:15-10:30 Session 5C Design Verification and Validation / Software Design for Testing
Chair: S. Fukumoto (Tokyo Metropolitan Univ.)
A Generalized Theory for Formal Assertion Coverage
S. Das (IIT Kharagpur), A. Banerjee (Indian Statistical Inst.), P. Dasgupta (IIT Kharagpur)
Error Model Free Automatic Design Error Correction of Complex Processors Using Formal
Methods
A. M. Gharehbaghi (JST), M. Fujita (Univ. Tokyo)
Hardware-Accelerated Workload Characterization for Power Modeling and Fault Injection
A. Krieg, J. Grinschgl, C. Steger, R. Weiss (Graz Univ.), H. Bock, J. Huid (Infineon Tech.),

10:50-12:30 Session 6A Temperature / Power-Aware Test II
Chair: H. Li (ICT/CAS)
Scan Test Power Simulation on GPGPUs
S. Holst, E. Schneider, H. -J. Wunderlich (Univ. Stuttgart)
Power Supply Noise Sensor based on Timing Uncertainty Measurements
M. Valka, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM), P. Debaud, S.
Guilhot (ST-Ericsson)
Peak Power Estimation: a Case Study on CPU Cores
P. Bernardi, M. D. Carvalho, E. Sanchez, M. S. Reorda (Politecnico di Torino), A. Bosio, L.
Dilillo, P. Girard, M. Valka (LIRMM)

Low Power BIST for Scan-Shift and Capture Power

10:50-12:30 Session 6B Analog Test and High-Speed I/O Test I
Chair: M. Hashizume (Univ. Tokushima)

Two-Tone Signal Generation for Communication Application ADC Testing
K. Kato, F. Abe, K. Wakabayashi, C. Gao, T. Yamada, H. Kobayashi (Gunma Univ.), O. Kobayashi (STARC), K. Niitsu (Gunma Univ.)

A New Procedure for Measuring High-Accuracy Probability Density Functions
T. J. Yamaguchi (Advantest), K. Asada (Univ. Tokyo), K. Niitsu (Gunma Univ.), M. Abbas, S. Komatsu (Univ. Tokyo), H. Kobayashi (Gunma Univ.), J. A. Moreira (Advantest)

Design of a High Bandwidth Interposer for Performance Evaluation of ATE Test Fixtures at the DUT Socket
J. Moreira (Advantest)

Spectral Estimation Based Acquisition of Incoherently Under-Sampled Periodic Signals: Application to Bandwidth Interleaving
D. Bhatta, N. Tzou (Georgia Inst. Tech.), H. Choi (Samsung), A. Chatterjee (Georgia Inst. Tech.)

10:50-12:30 Session 6C Board and System Test
Chair: K.-J. Lee (National Cheng Kung Univ.)

Board-Level Functional Fault Diagnosis Using Learning Based on Incremental Support-Vector Machines
F. Ye (Duke Univ.), Z. Zhang (Huawei Tech.), K. Chakrabarty (Duke Univ.), X. Gu (Huawei Tech.)

Adaptive Board-Level Functional Fault Diagnosis Using Decision Trees
F. Ye (Duke Univ.), Z. Zhang (Huawei Tech.), K. Chakrabarty (Duke Univ.), X. Gu (Huawei Tech.)

Reuse of Structural Volume Test Methods for In-System Testing of Automotive ASICs
A. Cook, D. Ull, M. Elm, H. J. Wunderlich (Univ. Stuttgart), H. Randolf, S. Dohren (Bosch)

13:30-15:10 Section 7A (Special Session 3)
Power-Aware Testing: Present and Future
Organizer: X. Wen (Kyushu Inst. Tech.)
Moderator: S.M. Reddy (Univ. Iowa)

Why and How Controlling Power Consumption During Test: A Survey
A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM)

PowerMAX: Fast Power Analysis during Test
W. Zhao, M. Tehranipoor (Univ. Connecticut)

Current and Future Directions in Automatic Test Pattern Generation for Power Delivery Network Validation
P. Varma (Apache Design)

Power-Supply Droop and Its Impacts on Structural At-Speed Testing
X. Lin (Mentor Graphics)

13:30-15:10 Section 7B
Special Session 4: Post-Silicon Measurements and Tests
Regular Session: Analog Test and High Speed I/O Test II
Organizer: T. J. Yamaguchi (Advantest)

(Special Session)
A Test Screening Method for 28nm HK/MG Single-port and Dual-port SRAMs Considering with Dynamic Stability and Read/Write Disturb Issues
K. Nii, Y. Tsukamoto, Y. Ishii, M. Yabuuchi, H. Fujiwara, K. Okamoto (Renesas)

Impact of All-Digital PLL on SoC Testing
T. Nakura, T. Iizuka, K. Asada (Univ. Tokyo)

(Regular Session)
Post-Silicon Jitter Measurements
K. Niitsu (Gunma Univ.), T. J. Yamaguchi, M. Ishida (Advantest), H. Kobayashi (Gunma Univ.)

An Active Test Fixture Approach for Testing 28 Gbps Applications Using a Lower Data Rate ATE System

13:30-15:10 Section 7C Panel: Board / System Test
Is Component Interconnection Test Enough for Board or System Test?
Panel Moderator: E. Larsson, (Lund Univ.)

Panelists:
X. Gu, (Huawei Tech.)
S. Kameyama, (Fujitsu)
M. Keim, (Mentor Graphics)
J. Qian, (AMD)
K. Chakrabarty, (Duke Univ.)

15:20 Social Program

Nov. 22nd, 2012

9:15-10:30 Session 8A Embedded Tutorial: Yield Analysis
Diagnosis for Accelerating Yield and Failure
Chair: K. S. -M. Li (National Sun Yat-sen Univ.)
W. -T. Cheng (Mentor Graphics), F. -M. Kuo (TSMC)

9:15-10:30 Session 8B Built-In Test and Built-In Characterization Technique
Chair: X. Li (ICT/CAS)
A Scan-Out Power Reduction Method for Multi-Cycle BIST
S. Wang, Y. Sato, K. Miyase, S. Kajihara (Kyushu Inst. Tech.)
A Test-Per-Clock LFSR Reseeding Algorithm for Concurrent Reduction on Test Sequence Length and Test Data Volume
W. -C. Lien, K. -J. Lee (National Cheng Kung Univ.), T. -Y. Hsieh (National Sun Yat-sen Univ.)
A Built-In Characterization Technique for 1-Bit/Stage Pipelined ADC
Y. -H. Chou, J. -L. Huang, X. -L. Huang (National Taiwan Univ.)

9:15-10:30 Session 8C ATPG
Chair: Y. Higami (Ehime Univ.)
Robust Timing-Aware Test Generation Using Pseudo-Boolean Optimization
S. Eggersgluess (Univ. Bremen), M. Yilmaz (NVIDIA), K. Chakrabarty (Duke Univ.)
Functional Pattern Generation for Asynchronous Designs in a Test Processor Environment
S. Zeidler, C. Wolf, M. Krstic, R. Kraemer (IHP)
Reduced-Complexity Transition-Fault Test Generation for Non-Scan Circuits through High-level Mutant Injection
V. Guarnieri, F. Fummi (Univ. Verona), K. Chakrabarty (Duke Univ.)

10:50-12:05 Session 9A Yield Analysis and Enhancement
Chair: S. -Y. Huang (National Tsing Hua Univ.)
Scrambling and Data Inversion Techniques for Yield Enhancement of NROM-Based ROMs
S. -K. Lu, T. -L. Li (National Taiwan Univ.), P. Ning (Nanya Tech.)
A Hybrid Flow for Memory Failure Bitmap Classification
J. Li (Tsinghua Univ.), Y. Huang, W. -T. Cheng, C. Schuermeyer (Mentor Graphics), D. Xiang (Tsinghua Univ.), E. Faehn (STMicroelectronics), R. Farrugia (STEricsson)
Test Cost Reduction for Performance Yield Recovery by Classification of Multiple-Clock Test Data
J. -H. Kuo, T. -S. Hsu, J. -J. Liou (National Tsing Hua Univ.)

10:50-12:05 Session 9B DFT / On-Line Test
Chair: P. Bernardi (Politecnico di Torino)
NoC Dynamically Reconfigurable as TAM
T. Sbiai, K. Namba (Chiba Univ.)
On-line Error Detection in Digital Microfluidic Biochips
D. Mitra (National Institute of Technology), S. Ghoshal, H. Rahaman (Bengal Engineering & Science Univ.), K. Chakrabarty (Duke Univ.), B. B. Bhattacharya (Indian Statistical Inst.)

Automatic Test Program Generation for Out-of-Order Superscalar Processors
Y. Zhang, A. Rezine, P. Ele, Z. Peng (Linkoping Univ.)

10:50-12:05 Session 9C Delay and Performance Test
Chair: Y. Sato (Kyushu Inst. Tech.)

Variation-Aware Fault Grading
A. Czutro (Univ. Freiburg), M. E. Imhot (Univ. Stuttgart), J. Jiang (Univ. Passau), A. Mumtaz (Univ. Stuttgart), M. Sauer, B. Becker (Univ. Freiburg), I. Polian (Univ. Passau), H. -J. Wunderlich (Univ. Stuttgart)

On-chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation
I. A. K. M. Mahfuzul, H. Onodera (Kyoto Univ.)

Efficient Trojan Detection via Calibration of Process Variations
B. Cha, S. K. Gupta (Univ. Southern California)
### Tutorial

**Nov. 19th, 2012**

**9:15-12:15 Tutorial 1**  
**Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliability**  
S. Venkataraman (Intel), R. Aitken (ARM)

**Summary:**  
The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

**Keywords:**  
Yield, Yield Modeling, Design-for-Manufacturability, Diagnosis, Design Margin, Yield Monitors, Variability and Reliability.

**13:45-16:45 Tutorial 2**  
**Power-Aware Testing and Test Strategies for Low Power Devices**  
P. Girard (LIRMM), N. Nicolici (McMaster Univ.), X. Wen (Kyushu Inst. Tech.)

**Summary:**  
Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability. EDA solutions for considering power during test and design-for-test are also discussed in the last part of the tutorial.

**Keywords:**  
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<td>• WRTLT'12</td>
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<td>• PRDC'12</td>
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## Visa Guide

Please check if you need an entry visa. It depends on your nationality, citizenship, etc. Please ask the nearest Japanese Embassy/Consulate ([http://www.mofa.go.jp/about/emb_cons/over/index.html](http://www.mofa.go.jp/about/emb_cons/over/index.html)) or please see the web site of The Ministry of Foreign Affairs of Japan: [http://www.mofa.go.jp/j_info/visit/visa/index.html](http://www.mofa.go.jp/j_info/visit/visa/index.html). ATS'12 Organizing Committee will provide the visa letters for this international symposium.

### Step 1:

Please fill this form ([ATS12_visa_request_form.docx](http://www.mofa.go.jp/about/emb_cons/over/index.html)) and send us by e-mail as soon as possible. This information is necessary to make your documents. We will prepare the necessary documents based on your information, and send them to you.

### Step 2:

Please submit the documents to the Japanese Embassy/Consulate ([http://www.mofa.go.jp/about/emb_cons/over/index.html](http://www.mofa.go.jp/about/emb_cons/over/index.html)). Then, you will receive the visa.

### Notice:

1. Visa letters will be issued only to:
   - Speakers / Presenters,
   - Committee Members,
   - Attendees who have paid their registration fee in full.
   (visa application should be submitted after his/her registration and payment process have been completed)

2. If you will be accompanied, please give us the necessary information about them. In general, you can apply for visas together, but in some cases you must apply separately. Please ask the nearest Japanese Embassy/Consulate.

3. Mailing visa documents (Step 1) often takes two or three weeks, and it can take more than one month for your visa application to be processed (Step 2). So, please send the form as soon as possible.

For inquiries, please contact Registration Chair (email: ats12-visa@aries30.cse.kyutech.ac.jp).
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The 21st Asian Test Symposium

November 19-22, 2012, Toki Messe Niigata Convention Center, Niigata, Japan

**SCOPE**

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind.

Major topics include, but are not limited to:

- Automatic Test Pattern Generation (ATPG)
- Analog Test / Mixed-Signal Test
- Boundary Scan Test
- Board and System Test
- Built-In Self-Test
- Design for Testability (DFT)
- Design Verification and Validation
- Defect-Based Testing
- Delay and Performance Test
- Diagnosis and Debug
- Dependable System
- Economics of Test
- Fault Modeling and Simulation
- Fault Tolerance
- High-Speed I/O Test / RF Testing
- Memory Test / FPGA Test
- On-Line Test
- System-on-a-Chip Test
- System-in-package (SiP)/ 3D Test
- Software Testing / Software Design for Testing
- Test Compression
- Temperature/Power-aware Test
- Test Quality
- Yield Analysis and Enhancement

**SUBMISSIONS**

Regular Session: The ATS’12 Program Committee invites original, unpublished paper submissions for ATS’12. A submission will be considered as evidence that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

Industry Session: This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The submission will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. Each submission should also include the complete address and designate a contact person and a presenter. Abstract submissions should be emailed to Industry Chair (ats12-industry@aries30.cse.kyutech.ac.jp).

Doctoral Thesis Award: The Award serves the purpose to promote most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology. This major Award is named after Prof. Edward J. McCluskey, a key educator and mentor in the fields of test technology. This major Award is named after Prof. Edward J. McCluskey, a key educator and mentor in the fields of test technology, logic design, and reliability. Call for paper of this award is available on the ATS2012 website (http://aries3a.cse.kyutech.ac.jp/~ats12/).

**KEY DATES (Regular Session)**

**Submission deadline:** June 15, 2012

(Submission site has been already closed.)

**Notification of acceptance:** Aug. 5, 2012

**Camera ready manuscript:** Aug. 31, 2012

**KEY DATES (Industry Session)**

**Submission deadline:** Jul. 19, 2012

**Notification of acceptance:** Aug. 5, 2012

**Camera ready manuscript:** Aug. 31, 2012

**KEY DATES (Dr. Thesis Award)**

**Submission deadline:** Aug. 20, 2012

**Notification of acceptance:** Sep. 20, 2012

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Program Chair: Hiroshi Takahashi
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The ATS'12 Program Committee invites original, unpublished paper submissions for ATS'12. Paper submissions should be complete manuscripts, up to six pages (including figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. An abstract of 50 words or less and 5-10 keywords are also required. All submissions are to be made electronically through the ATS'12 website. Detailed instructions for submissions are to be found at the ATS'12 website. Electronic submissions in PDF files are strongly recommended. A submission will be considered as evidence that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

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http://welcome.molesystems.com/ttc/ATS/2012/

**Key Dates (Regular Session)**

**Submission deadline:** May 25, 2012 --> June 10th, 2012 --> June 15th, 2012

Notification of acceptance: Aug. 5, 2012

Camera ready copy: Aug. 31, 2012

**Industry Session**

This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. Each submission should also include the complete address and designate a contact person and a presenter. Abstract submissions should be emailed to Industry Chair (ats12-industry@aries30.cse.kyutech.ac.jp).

**Key Dates (Industry Session)**

**Submission deadline:** Jul. 5, 2012 --> Jul. 19, 2012

Notification of acceptance: Aug. 5, 2012

Camera ready copy: Aug. 31, 2012
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- Program Committee
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The 21st Asian Test Symposium
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  Kuen-Jong Lee, National Cheng Kung University

• Members:
  Bhargab Bhattacharya, Indian Statistical Institute
  Krishnendu Chakrabarty, Duke University
  Serge Demidenko, Monash University
  Hideo Fujiwara, Osaka Gakuin University
  Patrick Girard, LIRMM / CNRS
  Shi-yu Huang, National Thing-Hua University
  Tomoo Inoue, Hiroshima City University
  Seiji Kajihara, Kyushu Institute of Technology
  Virendra Singh, Indian Institute of Science
  Chau-Chin Su, National Chiao Tung University
  Hiroshi Takahashi, Ehime University
  Shiyi Xu, Shanghai University
  Dafang Zhang, Hunan University
ATS Doctoral Thesis Award

Semi-Final of TTTC’s E.J. McCluskey Best Doctoral Thesis Award

The Doctoral Student Contest

- The contest is held in two stages: semi-finals and finals
- Asian semi-finals 2012 are held at ATS 2012 in Niigata, Japan
- The industrial jury and the academic jury will determine the winner
- The winner will compete against other regional winners in the finals at ITC 2013
- Both the student and the advisor of the winning work will be recognized

Eligibility

- Doctoral students working on test-related topics are eligible for the Award
- An individual can only participate in the contest once in a lifetime
- Student who graduated in 2012 or will graduate in 2013 are invited
- Participation is encouraged when the thesis is close to completion.
- Submissions to multiple regional sites are prohibited

Submission Instructions

- Contestants must submit a summary of their thesis work (up to 2000 words), beginning with the title of the thesis, the student’s name and affiliation, and the expected date of graduation
- One additional page is allowed for figures and references only.
- In addition, please submit an endorsement by the advisor (i.e. a statement that he/she supports the student’s participation in the contest with a signature
- The above contents must be included in one PDF file. Please use your first name plus last initial to name the PDF file.
- Contestants are free to submit up to three published papers in PDF version (named: Ref1.pdf, Ref2.pdf, Ref3.pdf), referenced as supporting materials
- All submissions must email to: viren@ee.iitb.ac.in, by September 05, 2012. (Extended)

The Semifinal

- Submissions will undergo a selection process
- Selected contestants, notified by September 20, will be given a short (about 6 minutes) presentation slot in a designated technical session at ATS’12
- The winner selected by the jury will be announced in the Banquet of ATS’12

Further Information

- ATS’12: http://aries3a.cse.kyutech.ac.jp/~ats12/
- Organizer: Virendra Singh, viren@ee.iitb.ac.in