ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convention Center, Niigata, Japan

Information

- Sponsor
- Scopes
- Submissions
- More Information

Registration

- Registration Procedure
- Accomodation Procedure
- Online Registration

ATS'12 Program

- ATS'12 at a Glance
- Advance Program
- Tutorial

Visa Guide

- Visa Guide

Conference Location

- The Venue

Call for Papers

- PDF

Paper Submission

- Regular Session
- Industry Session

Committees

- Organizing Committee

Information

Latest News!!

Online Registration has been closed!

Sponsored by

IEEE Computer Society Test Technology Technical Council
Kyushu Institute of Technology

In cooperation with

The IEICE Information and Systems Society Technical Committee on Dependable Computing
Japan Science and Technology Agency

Scopes

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind.

Major topics include, but are not limited to:

- Automatic Test Pattern Generation (ATPG)
- Analog Test / Mixed-Signal Test
- Boundary Scan Test
- Board and System Test
- Built-In Self-Test
- Design for Testability (DFT)
- Design Verification and Validation
- Defect-Based Testing
- Delay and Performance Test
- Fault Modeling and Simulation
- Fault Tolerance
- High-Speed I/O Test / RF Testing
- Memory Test / FPGA Test
- On-Line Test
- System-on-a-Chip Test
- System-in-package (SiP)/ 3D Test
- Software Testing / Software Design for Testing

- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

- Diagnosis and Debug
- Dependable System
- Economics of Test

Test Compression

- Temperature/Power-aware Test
- Test Quality
- Yield Analysis and Enhancement

Submissions

Regular Session:

The ATS'12 Program Committee invites original, unpublished paper submissions for ATS'12. Paper submissions should be complete manuscripts, up to six pages (including figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. **(For more details...)**

Key Dates (Regular Session)

Submission deadline: ~~**May 25, 2012 --> June 10th, 2012**~~ **--> June 15th, 2012**
Notification of acceptance: Aug. 5, 2012
Camera ready copy: Aug. 31, 2012

Industry Session:

This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. **(For more details...)**

Key Dates (Industry Session)

Submission deadline: ~~**Jul. 5, 2012**~~ **--> Jul. 19th, 2012**
Notification of acceptance: Aug. 5, 2012
Camera ready copy: Aug. 31, 2012

Doctoral Thesis Award:

The Award serves the purpose to promote most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology. This major Award is named after Prof. Edward J. McCluskey, a key educator and mentor in the fields of test technology, logic design, and reliability. **CFP(pdf)**

Key Dates (Doctoral Thesis Award)

Submission deadline: **Sep. 5th, 2012**
Notification of acceptance: Sep. 20, 2012

More Information

For general information
General Chair: Kazumi Hatayama (ats12-gc@aries30.cse.kyutech.ac.jp)

For submission related information
Program Chair: Hiroshi Takahashi (ats12-pc@aries30.cse.kyutech.ac.jp)

ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convention Center, Niigata, Japan

Information

- Sponsor
- Scopes
- Submissions
- More Information

Registration

- Registration Procedure
- Accomodation Procedure
- Online Registration

ATS'12 Program

- ATS'12 at a Glance
- Advance Program
- Tutorial

Visa Guide

- Visa Guide

Conference Location

- The Venue

Call for Papers

- PDF

Paper Submission

- Regular Session
- Industry Session

Committees

- Organizing Committee

Information

Latest News!!

Online Registration has been closed!

Sponsored by

IEEE Computer Society Test Technology Technical Council
Kyushu Institute of Technology

In cooperation with

The IEICE Information and Systems Society Technical Committee on Dependable Computing
Japan Science and Technology Agency

Scopes

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind.

Major topics include, but are not limited to:

- Automatic Test Pattern Generation (ATPG)
- Analog Test / Mixed-Signal Test
- Boundary Scan Test
- Board and System Test
- Built-In Self-Test
- Design for Testability (DFT)
- Design Verification and Validation
- Defect-Based Testing
- Delay and Performance Test
- Fault Modeling and Simulation
- Fault Tolerance
- High-Speed I/O Test / RF Testing
- Memory Test / FPGA Test
- On-Line Test
- System-on-a-Chip Test
- System-in-package (SiP)/ 3D Test
- Software Testing / Software Design for Testing

- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

- Diagnosis and Debug
- Dependable System
- Economics of Test

Test Compression

- Temperature/Power-aware Test
- Test Quality
- Yield Analysis and Enhancement

Submissions

Regular Session:

The ATS'12 Program Committee invites original, unpublished paper submissions for ATS'12. Paper submissions should be complete manuscripts, up to six pages (including figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. **(For more details...)**

Key Dates (Regular Session)

Submission deadline: ~~**May 25, 2012 --> June 10th, 2012**~~ **--> June 15th, 2012**
Notification of acceptance: Aug. 5, 2012
Camera ready copy: Aug. 31, 2012

Industry Session:

This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. **(For more details...)**

Key Dates (Industry Session)

Submission deadline: ~~**Jul. 5, 2012**~~ **--> Jul. 19th, 2012**
Notification of acceptance: Aug. 5, 2012
Camera ready copy: Aug. 31, 2012

Doctoral Thesis Award:

The Award serves the purpose to promote most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology. This major Award is named after Prof. Edward J. McCluskey, a key educator and mentor in the fields of test technology, logic design, and reliability. **CFP(pdf)**

Key Dates (Doctoral Thesis Award)

Submission deadline: Sep. 5th, 2012
Notification of acceptance: Sep. 20, 2012

More Information

For general information
General Chair: Kazumi Hatayama (ats12-gc@aries30.cse.kyutech.ac.jp)

For submission related information
Program Chair: Hiroshi Takahashi (ats12-pc@aries30.cse.kyutech.ac.jp)

IEEE Asian Test Symposium 2012

Registration Application Procedures

Registration Fee

Category	Early Registration (on and before October 18, 2012)	Late Registration (on and after October 19, 2012)
Symposium (Members)	JPY 45,000	JPY 54,000
Symposium (Non-members)	JPY 57,000	JPY 69,000
Symposium (Student/Life/Retired members)	JPY 11,000	JPY 13,000
Symposium (Student non-members)	JPY 14,000	JPY 17,000
Symposium 1st-day-only [Nov.20] (Members)	JPY 27,000	JPY 27,000
Symposium 1st-day-only [Nov.20] (Non-members)	JPY 34,000	JPY 34,000
Tutorial Full Day (Members)	JPY 23,000	JPY 30,000
Tutorial Full Day (Non-members)	JPY 32,000	JPY 42,000
Tutorial Full Day Ohters (Students/Life/Retired)	JPY 13,000	JPY 17,000
Tutorial Half Day (Members)	JPY 14,000	JPY 18,000
Tutorial Half Day (Non-members)	JPY 18,000	JPY 25,000
Tutorial Half Day Others (Students/Life/Retired)	JPY 9,000	JPY 11,000

*Extra social event tickets JPY10,000

Registration fee includes:

Symposium (Members)	proceedings social event (reception on Nov.19, tour, banquet on Nov.21)
Symposium (Non-members)	proceedings social event (reception on Nov.19, tour, banquet on Nov.21)
Symposium (Student/Life/Retired members)	proceedings
Symposium (Student non-members)	proceedings
Symposium 1st-day-only [Nov.20] (Members)	proceedings reception on Nov. 19
Symposium 1st-day-only [Nov.20] (Non-members)	proceedings reception on Nov. 19

*IEEE member rate is also applied for IEICE members.
*Registration fee for IEEE member and Non-member includes social event tickets.
*Student/Life/Retired member fees do not include the social event (the reception, the tour and the banquet).
*At least one author must register with the paper reference number by September 7.
*Participant lists including name, affiliation, and country will be distributed to attendees.
*If you need to cancel or edit, please contact westec_op13@west.jtb.jp

*Only be issued a receipt in full amount of registration (Include:social event ticket, extra ticket)
If you need a receipt of hotel, please contact westec_op13@west.jtb.jp
*If you need change of item about receipt, Please contact westec_op13@west.jtb.jp
*We will pass ireceipt at the venue on the day.

For domestic participants:
日本の方はお支払いの際、銀行振込にて御願いいたします。
会議の運営経費削減にご協力ください。

Registration Procedure

Please complete your registration by logging-in to your "My Page".
If you have not yet registered your personal information, please first complete the required items on the ID Application page in order to obtain a log-in ID and Password.

Payment Procedure

After you complete your reservation, please click the "Full Payment" button displayed on the Payment Status page.
Credit Card payment, Convenience Store payment, Pay-easy are acceptable for the Symposium. In order to make your reservation, a full deposit will be necessary. Payment must be made latest on or before 5 November, 2012.

[How to pay by credit card]
The credit cards listed below can be used to make payments.

Visa, MasterCard®, JCB, AMEX, Dinners Club

1. For VISA, Master Card®, and JCB cardholders

This system supports 3-D Secure for certain cardholders in order to provide a more secure online payment experience.

What is 3-D Secure?
This system adds an authentication step to the online payment process by requiring the user to enter a previously registered password on an authentication screen provided by the credit card issuer. International credit card brands VISA, MasterCard®, and JCB recommend that merchants make use of this system.

Credit card issuers use different names to refer to their implementation of 3-D Secure, including Verified by VISA (used by VISA), MasterCard® SecureCode™ (MasterCard®), and J/Secure™ (JCB).

*Some issuers allow cardholders to use the same password they have been assigned for accessing their monthly statements online or having them sent by email. If this password is not entered, or if an incorrect password is entered, the online transaction will not be completed.

*If you forget your password or experience other authentication-related issues, please contact your credit card issuer. (For more information, see your credit card issuer's website.)

*In terms of the actual payment process, once you have entered your card information (issuer, card number, expiration date, and cardholder name), click the "Next" button to proceed to the credit card issuer's authentication screen.

2. For AMERICAN EXPRESS (AMEX) and Diners Club International cardholders

Card number, expiration date and security code will be required for the payment.

*The security code is the last 3 digits of the number printed above the card holder signature area on the back of the card.

*For American Express cards, this is the 4 digits number stamped above the card number on the front of the card.

For more details on the credit card payment, please refer to *About Payment* on My Page.

For domestic participants:
日本の方はお支払いの際、銀行振込にて御願いいたします。
会議の運営経費削減にご協力ください。

*銀行振込で手順がご不明な場合は、JTBまでご連絡をお願い致します。（westec_op13@west.jtb.jp）
お振込先情報をお送りさせていただきます。
*銀行振込の際のお振込手数料はご参加者様負担となりますので、予めご了承お願いいたします。
*銀行振り込みの送金の期限は、10月25日までです。参加登録後、1週間以内にお振込お願い致します。
*Early Registration期間中にお振込が確認できない場合は、Late Registrationの料金が適用されますので、ご注意ください。
*WEB上での事前参加受付けの終了後は、当日現金にてお支払いただきます。

Confirmation

Your registration will be completed upon receipt of your on-line registration information and payment.
A "Confirmation sheet" button will be displayed when you complete your registration.
Please print out your confirmation slip by clicking the "Confirmation sheet" button and bring it with you to the On-site Registration Desk.

Cancellation

*In case of cancellation, your registration fee will be refunded after deducting the cancellation fees as shown below.
*Please note all refunds will be made after the the Conference/the Symposium.

Cancellation Fee

On or Before October 18	JPY 5,000
On or After October 19	100% of the registration fee/No refund

If you wish to cancel your registration, please contact westec_op13@west.jtb.jp.

Deadline for Registration

The deadline for online registration is

23:59 of November 5, 2012, Japan Standard Time (GMT+9)

Inquiries for Registration

Please send us your inquiries by logging-in to your "My Page" and clicking on the "Inquiry" button.

JTB Western Japan Corp.,
MICE Center
IEEE Asian Test Symposium 2012

TEL: +81-6-6252-2861
FAX: +81-6-6252-2862
E-mail: westec_op13@west.jtb.jp
Office hours: 9:30-17:30 (weekdays only)

Close

Accommodations Application Procedures

General Information

JTB Western Japan Corp. (JTB) has been appointed as an official travel agent for the Conference and will handle hotel accommodations.
Hotel assignment will be made on a first-come, first-served basis.
*Please check the hotel list for details of accommodations.
*Rates are valid for the stay from November 18, 19, 20, 21, 22, to 23 2012
*The hotel rates are per person, per night, including service charge and consumption tax with Breakfast.
*All guests are required to make own arrangements to the hotel from airports or railway stations.
*Minimum number required is 1 person.

HOTEL MAP

Hotel Information

*Please click on each hotel name to confirm hotel information.
*You can check hotel fees of each day or room type by clicking on "Room Rate".

Hotel Name	Room Type, Number of Person(s), etc.	Room Rate
1.Hotel Nikko Niigata	Single room 1 person(s) with breakfast	JPY10,500 Room Rate
	Twin room 1 person(s) to 2 person(s) with breakfast	JPY9,500 to JPY15,500 Room Rate
2.ANA Crowne Plaza Hotel Niigata	Single room 1 person(s) with breakfast	JPY12,050 Room Rate
	Twin room 1 person(s) to 2 person(s) with breakfast	JPY9,975 to JPY14,700 Room Rate
3.Niigata Tokyu Inn	Single room 1 person(s) with breakfast	JPY7,900 Room Rate
	Twin room 1 person(s) to 2 person(s) with breakfast	JPY6,900 to JPY10,400 Room Rate
4.Niigata Daiichi Hotel	Single room 1 person(s) with breakfast	JPY6,850 Room Rate
	Twin room 1 person(s) to 2 person(s) with breakfast	JPY6,450 to JPY9,050 Room Rate
5.Niigata Station Hotel	Single room 1 person(s) with breakfast	JPY6,800 Room Rate
	Twin room 1 person(s) to 2 person(s) with breakfast	JPY6,275 to JPY7,850 Room Rate

Reservation Procedure

Please complete your reservation by logging-in to your "My Page".
*If you have not yet registered your personal information, please first complete the required items on the ID Application page in order to obtain a log-in ID and Password.

Payment Procedure

After you complete your reservation, please click the "Full Payment" button displayed on the Payment Status page.
Credit Card payment, Convenience Store payment, Pay-easy are acceptable for the Symposium. In order to make your reservation, a full deposit

will be necessary. Payment must be made latest on or before 5 November, 2012.

[How to pay by credit card]
The credit cards listed below can be used to make payments.

Visa, MasterCard®, JCB, AMEX, Dinners Club

1. For VISA, Master Card®, and JCB cardholders

This system supports 3-D Secure for certain cardholders in order to provide a more secure online payment experience.

What is 3-D Secure?
This system adds an authentication step to the online payment process by requiring the user to enter a previously registered password on an authentication screen provided by the credit card issuer. International credit card brands VISA, MasterCard®, and JCB recommend that merchants make use of this system.

Credit card issuers use different names to refer to their implementation of 3-D Secure, including Verified by VISA (used by VISA), MasterCard® SecureCode™ (MasterCard®), and J/Secure™ (JCB).

*Some issuers allow cardholders to use the same password they have been assigned for accessing their monthly statements online or having them sent by email. If this password is not entered, or if an incorrect password is entered, the online transaction will not be completed.

*If you forget your password or experience other authentication-related issues, please contact your credit card issuer. (For more information, see your credit card issuer's website.)

*In terms of the actual payment process, once you have entered your card information (issuer, card number, expiration date, and cardholder name), click the "Next" button to proceed to the credit card issuer's authentication screen.

2. For AMERICAN EXPRESS (AMEX) and Diners Club International cardholders

Card number, expiration date and security code will be required for the payment.

*The security code is the last 3 digits of the number printed above the card holder signature area on the back of the card.

*For American Express cards, this is the 4 digits number stamped above the card number on the front of the card.

For more details on the credit card payment, please refer to *About Payment* on My Page.

*If you would like to pay by bank transfer, please contact westec_op13@west.jtb.jp
*In case of bank transfer, a remittance fee will be added to your remittance form.
*If you need change of item about receipt, Please contact westec_op13@west.jtb.jp

Confirmation

The Confirmation button will be displayed when you complete your reservation. Please print your confirmation slip by clicking the Confirmation button and bring it with you to the reception desk upon checking-in at the hotel.

Cancellation / Revision

*In case of cancellation, your deposit will be refunded after deducting the cancellation fees as follows.
*Please revise and/or cancel your reservation by logging-in to your "My Page".
*Cancellation fee when notice is given

8 days or more days prior to the first night of stay･･･0% of daily room rate
2 to 7 days before the first night of stay････20% of daily room rate
1 day before the first night of stay････40% of daily room rate
The first night of stay if notice given before noon(Japan Time) on check-in day･･･50% of daily room rate

The first night of stay if no notice given･･･100% of daily room rate

Deadline for Accommodations

The deadline for Reservations on this site is
23:59 of November 5, 2012 Japan Standard Time (GMT+9)
(Please note that reservations will also be closed when all the accommodations have become full.)

Inquiries for Accommodations

Please send us your inquiries by logging-in to your "My Page" and clicking on the "Inquiry" button.

JTB Western Japan Corp.,
MICE Center
IEEE Asian Test Symposium 2012

TEL: +81-6-6252-2861
FAX: +81-6-6252-2862
E-mail: westec_op13@west.jtb.jp
Office hours: 9:30-17:30 (weekdays only)

閉じる

v.9.31
ServerName:JW001

ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convetion Center, Niigata, Japan

Information

- Sponsor
- Scopes
- Submissions
- More Information

Registration

- Registration Procedure
- Accomodation Procedure
- Online Registration

ATS'12 Program

- ATS'12 at a Glance
- Advance Program
- Tutorial

Visa Guide

- Visa Guide

Conference Location

- The Venue

Call for Papers

- PDF

Paper Submission

- Regular Session
- Industry Session

Committees

ATS'12 at a Glance

		Room 302 A/B	Room 301 A	Room 301 B
Nov.19 (Mon.)	9:15-12:15	Tutorial 1 (Room 301 B)		
	12:15-13:45	Lunch Time		
	13:45-16:45	Tutorial 2 (Room 301 B)		
	18:00-	Welcome Reception (Hotel Nikko Niigata 4F)		
Nov.20 (Tue.)	9:30-10:40	Plenary Session 1 (Marine Hall)		
	10:40-11:00	Coffee Break		
	11:00-12:20	Plenary Session 2 (Marine Hall)		
	12:20-13:40	Lunch Time		
	13:40-15:20	3A Industry Session **13:40-14:40 Oral @ 302A/B 14:40-15:40 Poster@ Foyer**	3B Diagnosis and Debug	3C System-in-Package (SiP)/3D IC Test
	15:20-15:40	Coffee Break		
	15:40-17:20	4A (Special Session 1) Quantum Informatics	4B (Special Session 2) Dependable VLSI	4C Test Compaction/Test Quality
	9:15-10:30	5A Temperature / Power-Aware Test I	5B Dependable Systems/Memory Test	5C Design Verification and Validation/Software Design for Testing
	10:30-10:50	Coffee Break		
	10:50-12:30	6A Temperature / Power-Aware Test II	6B Analog Test and High-Speed I/O Test I	6C Board and System Test

- Organizing Committee
- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

Nov.21 (Wed.)				
	12:30- 13:30	Lunch Time		
	13:30- 15:10	7A(Special Session 3) Power-Aware Testing: Present and Future	7B(Special Session 4) Post-Silicon Measurements and Tests /Analog Test and High-Speed I/O Test II	7C Panel: Boad / System Test
	15:20- 22:00	Social Program		
Nov.22 (Thu)	9:15- 10:30	8A Embedded Tutorial Yield Analysis	8B Built-In Test and Built-In Characterization Technique	8C ATPG
	10:30- 10:50	Coffee Break		
	10:50- 12:05	9A Yield Analysis and Enhancement	9B DFT/On-Line Test	9C Delay and Performance Test

ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convetion Center, Niigata, Japan

Information

- Sponsor
- Scopes
- Submissions
- More Information

Registration

- Registration Procedure
- Accomodation Procedure
- Online Registration

ATS'12 Program

- ATS'12 at a Glance
- Advance Program
- Tutorial

Visa Guide

- Visa Guide

Conference Location

- The Venue

Call for Papers

- PDF

Paper Submission

- Regular Session
- Industry Session

Committees

ATS'12 Advance Program

Jump to November 19th, 20th, 21st, 22nd

Nov. 19th, 2012

9:15-12:15 Tutorial 1

Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliability
S. Venkataraman (Intel), R. Aitken (ARM)

13:45-16:45 Tutorial 2

Power-Aware Testing and Test Strategies for Low Power Devices
P. Girard (LIRMM), N. Nicolici (McMaster Univ.), X. Wen (Kyushu Inst. Tech.)

Nov. 20th, 2012

9:30-10:40 Plenary Session 1

Keynote Address I:
On-Chip Sensors to Support Parametric Test and Diagnosis
J. A. Abraham (Univ. Texas)

Keynote Address II:
VLSI Design and Testing for Enhanced Systems Dependability
S. Asai (CREST and Rigaku Corp.)

11:00-12:20 Plenary Session 2

Invited Talk I:
3-D Integration Technology and Future Trend
M. Koyanagi (Tohoku Univ.)

Invited Talk II:
Next-Generation Testing: Towards a New Level of Abstraction
P. Wohl (Synopsys)

13:40-15:40 Session 3A (Industry Session)

13:40-14:40 Oral Presentation
14:40-15:40 Poster Presentation

An Effective At-speed Scan Testing Approach Using Multiple-Timing Clock Waveforms
H. Iwata, Y. Maeda, J. Matsushima, M. Takakura (Renesas)

LBIST/ATPG technologies used for on-demand digital logic testing in Automotive Circuits

- Organizing Committee
- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

D. Meehl, B. Petrakis, P. Zhang (Cadence)

Portable/Desktop Testing Solution for Engineering with Cloud
N. Takahashi, T. Watanabe, T. Suzuki, M. Kimura (Advantest)

Characteristics Variability Evaluation of Actual LSI Transistors with Nanoprobing
M. Fukui, Y. Nara, J. Fuse (Hitach High-Tech.)

F-matrix (ABCD-matrix) Circuit Simulation Built in IC Test Program
H. Okawara (Advantest)

Addressing Test Challenges in Advanced Technology Nodes
Y. Zorian (Synopsys)

13:40-15:20 Session 3B Diagnosis and Debug

Chair: H. -J Wunderlich (Univ. Stuttgart)

Diagnosis of Cell Internal Defects With Multi-Cycle Test Patterns
X. Fan (Univ. Iowa), M. Sharama, W. -T. Cheng (Mentor Graphics), S. M. Reddy (Univ. Iowa)

Automated Post-Silicon Debugging of Failing Speedpaths
M. Dehbashi (Univ. Bremen), G. Fey (German Aerospace Genter)

SAT-based automatic rectification and debugging of combinational circuits with LUT insertions
S. Jo, T. Matsumoto, M. Fujita (Univ. Tokyo)

A new look ahead technique for customized testing in Digital Microfluidic Biochips
P. Roy, H. Rahaman (Bengal Engineering and Science Univ.), P. Dasgupta (Indian Inst. Management)

13:40-15:20 Session 3C System-in-Package (SiP) / 3D IC Test

Chair: D. Xiang (Tsinghua Univ.)

TSV Stress-Aware ATPG for 3D Stacked ICs
S. Deutsch, K. Chakrabarty (Duke Univ.), S. Panth, S. K. Lim (Georgia Inst. Tech.)

Linear Programming Formulations for Thermal-Aware Test-Scheduling of 3D-Stacked Integrated Circuits
S. K. Millican, K. K. Saluja (Univ. Wisconsin)

Programmable Leakage Test and Binning for TSVs
Y. -H. Lin, S. -Y. Huang (National Tsing Hua Univ.), K. -H. Tsai, W. -T. Cheng (Mentor Graphics)

15:40-17:20 Session 4A (Special Session 1)
Quantum Informatics: Classical Circuit Synthesis, Resource Optimisation and Benchmarking

Organizer: Ilia Polian (Univ. Passau)

Counting Gates, Moving Qubits: Evaluating the Execution Cost of Quantum Circuits
R. V. Meter (Keio Univ.)

Programming a Topological Quantum Computer
S. Devitt, K. Nemoto (National Inst. Info.)

An Optimization Problem for Topological Quantum Computation
S. Yamashita (Ritsumeikan Univ.)

Classical challenge problems to realise a surface code quantum computer
A. Fowler (Univ. Melbourne)

15:40-17:20 Session 4B (Special Session 2)
Dependable VLSI

Organizer: X. Gu (Huawei Tech.)

Soft Error Issues with Scaling Technologies
S. Baeg, J. Bae, S. Lee, C. S. Lim, S. H. Jeon, H. Lee (Hanyang Univ.)

In-field Testing of NAND Flash Storage: Why and How?
Y. Hu (ICT/CAS), X. Gu (Huawei Tech.), X. Li (ICT/CAS)

A Few Design Techniques for "Dependability" of an SOC
J. Qian (AMD)

Accessing Embedded DfT Instruments with IEEE P1687

E. Larsson (Lund Univ.), F. G. Zadegan (Linkoping Univ.)

15:40-17:20 Session 4C Test Compaction / Test Quality
Chair: T. Hosokawa (Nihon Univ.)

Multi-Level EDT to Reduce Scan Channels in SoC Designs
G. Li, J. Qian, P. Li, G. Zuo (AMD)

On Utilizing Test Cube Properties to Reduce Test Data Volume Further
X. Lin, J. Rajski (Mentor Graphics)

Note on Layout-Aware Weighted Probabilistic Bridge Fault Coverage
M. Arai, Y. Shimizu, K. Iwasaki (Tokyo Metropolitan Univ.)

Tailoring Tests for Functional Binning of Integrated Circuits
S. Sindia, V. D. Agrawal (Auburn Univ.)

Nov. 21st, 2012

9:15-10:30 Session 5A Temperature / Power-Aware Test I
Chair: M. Yoshimura (Kyushu Univ.)

A Thermal-Driven Test Application Scheme for 3-Dimensional ICs
D. Xiang, K. Shen, Y. Deng (Tsinghua Univ.)

A Transition Isolation Scan Cell Design for Low Shift and Capture Power
Y. -T. Lin, J. -L. Huang (National Taiwan Univ.), X. Wen (Kyushu Insti. Tech.)

A Probabilistic and Constraint Based Approach for Low Power Test Generation
H. Sabaghian-Bidgoli, M. Namaki-Shoushtari, Z. Navabi (Univ. Tehran)

9:15-10:30 Session 5B Dependable Systems / Memory Test
Chair: S. Gupta (Univ. Southern California)

Dual Edge Triggered Flip-Flops for Noise Blocking and Application to Signal Delay Detection
Y. Ohkawa, Y. Miura (Tokyo Metropolitan Univ.)

Impact of Resistive-Bridge Defects in TAS-MRAM Architectures
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri (LIRMM), G. Prenat CEA/SPINTEC), J. Alvarez-Herault, K. Mackay (CROCUS Tech.)

SoftPCM: Enhancing Energy Efficiency and Lifetime of Phase Change Memory in Video Applications via Approximate Write
Y. Fang, H. Li, X. Li (ICT/CAS)

9:15-10:30 Session 5C Design Verification and Validation / Software Design for Testing
Chair: S. Fukumoto (Tokyo Metropolitan Univ.)

A Generalized Theory for Formal Assertion Coverage
S. Das (IIT Kharagpur), A. Banerjee (Indian Statistical Inst.), P. Dasgupta (IIT Kharagpur)

Error Model Free Automatic Design Error Correction of Complex Processors Using Formal Methods
A. M. Gharehbaghi (JST), M. Fujita (Univ. Tokyo)

Hardware-Accelerated Workload Characterization for Power Modeling and Fault Injection
A. Krieg, J. Grinschgl, C. Steger, R. Weiss (Graz Univ.), H. Bock, J. Haid (Infineon Tech.),

10:50-12:30 Session 6A Temperature / Power-Aware Test II
Chair: H. Li (ICT/CAS)

Scan Test Power Simulation on GPGPUs
S. Holst, E. Schneider, H. -J. Wunderlich (Univ. Stuttgart)

Power Supply Noise Sensor based on Timing Uncertainty Measurements
M. Valka, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM), P. Debaud, S. Guilhot (ST-Ericsson)

Peak Power Estimation: a Case Study on CPU Cores
P. Bernardi, M. D. Carvalho, E. Sanchez, M. S. Reorda (Politecnico di Torino), A. Bosio, L. Dilillo, P. Girard, M. Valka (LIRMM)

Low Power BIST for Scan-Shift and Capture Power
Y. Sato, S. Wang, T. Kato, K. Miyase, S. Kajihara (Kyushu Inst. Tech.)

10:50-12:30 Session 6B Analog Test and High-Speed I/O Test I

Chair: M. Hashizume (Univ. Tokushima)

Two-Tone Signal Generation for Communication Application ADC Testing
K. Kato, F. Abe, K. Wakabayashi, C. Gao, T. Yamada, H. Kobayashi (Gunma Univ.), O. Kobayashi (STARC), K. Niitsu (Gunma Univ.)

A New Procedure for Measuring High-Accuracy Probability Density Functions
T. J. Yamaguchi (Advantest), K. Asada (Univ. Tokyo), K. Niitsu (Gunma Univ.), M. Abbas, S. Komatsu (Univ. Tokyo), H. Kobayashi (Gunma Univ.), J. A. Moreira (Advantest)

Design of a High Bandwidth Interposer for Performance Evaluation of ATE Test Fixtures at the DUT Socket
J. Moreira (Advantest)

Spectral Estimation Based Acquisition of Incoherently Under-Sampled Periodic Signals : Application to Bandwidth Interleaving
D. Bhatta, N. Tzou (Georgia Inst. Tech.), H. Choi (Samsung), A. Chatterjee (Georgia Inst. Tech.)

10:50-12:30 Session 6C Board and System Test

Chair: K. -J. Lee (National Cheng Kung Univ.)

Board-Level Functional Fault Diagnosis Using Learning Based on Incremental Support-Vector Machines
F. Ye (Duke Univ.), Z. Zhang (Huawei Tech.), K. Chakrabarty (Duke Univ.), X. Gu (Huawei Tech.)

Adaptive Board-Level Functional Fault Diagnosis Using Decision Trees
F. Ye (Duke Univ.), Z. Zhang (Huawei Tech.), K. Chakrabarty (Duke Univ.), X. Gu (Huawei Tech.)

Reuse of Structural Volume Test Methods for In-System Testing of Automotive ASICs
A. Cook, D. Ull, M. Elm, H. -J. Wunderlich (Univ. Stuttgart), H. Randoll, S. Dohren (Bosch)

13:30-15:10 Section 7A (Special Session 3)
Power-Aware Testing: Present and Future

Organizer: X. Wen (Kyushu Inst. Tech.)
Moderator: S.M. Reddy (Univ. Iowa)

Why and How Controlling Power Consumption During Test: A Survey
A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM)

PowerMAX: Fast Power Analysis during Test
W. Zhao, M. Tehranipoor (Univ. Connecticut)

Current and Future Directions in Automatic Test Pattern Generation for Power Delivery Network Validation
P. Varma (Apache Design)

Power-Supply Droop and Its Impacts on Structural At-Speed Testing
X. Lin (Mentor Graphics)

13:30-15:10 Section 7B
Special Session 4: Post-Silicon Measurements and Tests
Regular Session: Analog Test and High Speed I/O Test II

Organizer: T. J. Yamaguchi (Advantest)

(Special Session)
A Test Screening Method for 28nm HK/MG Single-port and Dual-port SRAMs Considering with Dynamic Stability and Read/Write Disturb Issues
K. Nii, Y. Tsukamoto, Y. Ishii, M. Yabuuchi, H. Fujiwara, K. Okamoto (Renesas)

Impact of All-Digital PLL on SoC Testing
T. Nakura, T. Iizuka, K. Asada (Univ. Tokyo)

(Regular Session)
Post-Silicon Jitter Measurements
K. Niitsu (Gunma Univ.), T. J. Yamaguchi, M. Ishida (Advantest), H. Kobayashi (Gunma Univ.)

An Active Test Fixture Approach for Testing 28 Gbps Applications Using a Lower Data Rate ATE System

J. Moreira, B. Roth, C. McCowan (Advantest)

13:30-15:10 Section 7C Panel: Board / System Test Is Componet Interconnection Test Enough for Board or System Test?

Panel Moderator: E. Larsson, (Lund Univ.)

Panelists:
X. Gu, (Huawei Tech.)
S. Kameyama, (Fujitsu)
M. Keim, (Mentor Graphics)
J. Qian, (AMD)
K. Chakrabarty, (Duke Univ.)

15:20 Social Program

Nov. 22nd, 2012

9:15-10:30 Session 8A Embedded Tutorial: Yield Analysis

Diagnosis for Accelerating Yield and Failure
Chair: K. S. -M. Li (National Sun Yat-sen Univ.)

W. -T. Cheng (Mentor Graphics), F. -M. Kuo (TSMC)

9:15-10:30 Session 8B Built-In Test and Built-In Characterization Technique

Chair: X. Li (ICT/CAS)

A Scan-Out Power Reduction Method for Multi-Cycle BIST
S. Wang, Y. Sato, K. Miyase, S. Kajihara (Kyushu Inst. Tech.)

A Test-Per-Clock LFSR Reseeding Algorithm for Concurrent Reduction on Test Sequence Length and Test Data Volume
W. -C. Lien, K. -J. Lee (National Cheng Kung Univ.), T. -Y. Hsieh (National Sun Yat-sen Univ.)

A Built-In Characterization Technique for 1-Bit/Stage Pipelined ADC
Y.-H. Chou, J. -L. Huang, X. -L. Huang (National Taiwan Univ.)

9:15-10:30 Session 8C ATPG

Chair: Y. Higami (Ehime Univ.)

Robust Timing-Aware Test Generation Using Pseudo-Boolean Optimization
S. Eggersgluess (Univ. Bremen), M. Yilmaz (NVIDIA), K. Chakrabarty (Duke Univ.)

Functional Pattern Generation for Asynchronous Designs in a Test Processor Environment
S. Zeidler, C. Wolf, M. Krstic, R. Kraemer (IHP)

Reduced-Complexity Transition-Fault Test Generation for Non-Scan Circuits through High-level Mutant Injection
V. Guarnieri, F. Fummi (Univ. Verona), K. Chakrabarty (Duke Univ.)

10:50-12:05 Session 9A Yield Analysis and Enhancement

Chair: S. -Y. Huang (National Tsing Hua Univ.)

Scrambling and Data Inversion Techniques for Yield Enhancement of NROM-Based ROMs
S. -K. Lu, T. -L. Li (National Taiwan Univ.), P. Ning (Nanya Tech.)

A Hybrid Flow for Memory Failure Bitmap Classification
J. Li (Tsinghua Univ.), Y. Huang, W. -T. Cheng, C. Schuermyer (Mentor Graphics), D. Xiang (Tsinghua Univ.), E. Faehn (STMicroelectronics), R. Farrugia (STEricsson)

Test Cost Reduction for Performance Yield Recovery by Classification of Multiple-Clock Test Data
J. -H. Kuo, T. -S. Hsu, J. -J. Liou (National Tsing Hua Univ.)

10:50-12:05 Session 9B DFT / On-Line Test

Chair: P. Bernardi (Politecnico di Torino)

NoC Dynamically Reconfigurable as TAM
T. Sbiai, K. Namba (Chiba Univ.)

On-line Error Detection in Digital Microfluidic Biochips
D. Mitra (National Institute of Technology), S. Ghoshal, H. Rahaman (Bengal Engineering & Science Univ.), K. Chakrabarty (Duke Univ.), B. B. Bhattacharya (Indian Statistical Inst.)

Automatic Test Program Generation for Out-of-Order Superscalar Processors
Y. Zhang, A. Rezine, P. Eles, Z. Peng (Linkoping Univ.)

10:50-12:05 Session 9C Delay and Performance Test

Chair: Y. Sato (Kyushu Inst. Tech.)

Variation-Aware Fault Grading
A. Czutro (Univ. Freiburg), M. E. Imhot (Univ. Stuttgart), J. Jiang (Univ. Passau), A. Mumtaz (Univ. Stuttgart), M. Sauer, B. Becker (Univ. Freiburg), I. Polian (Univ. Passau), H. -J. Wunderlich (Univ. Stuttgart)

On-chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation
I. A. K. M. Mahfuzul, H. Onodera (Kyoto Univ.)

Efficient Trojan Detection via Calibration of Process Variations
B. Cha, S. K. Gupta (Univ. Southern California)

ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convetion Center, Niigata, Japan

---

Information

- Sponsor
- Scopes
- Submissions
- More Information

Registration

- Registration Procedure
- Accomodation Procedure
- Online Registration

ATS'12 Program

- ATS'12 at a Glance
- Advance Program
- Tutorial

Visa Guide

- Visa Guide

Conference Location

- The Venue

Call for Papers

- PDF

Paper Submission

- Regular Session
- Industry Session

Committees

Tutorial

Nov. 19th, 2012

9:15-12:15 Tutorial 1

Beyond DFT: The Convergence of DFM, Variability, Yield, Diagnosis and Reliability

S. Venkataraman (Intel), R. Aitken (ARM)

Summary:
The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

Keyworks:
Yield, Yield Modeling, Design-for-Manufacturability, Diagnosis, Design Margin, Yield Monitors, Variability and Reliability.

13:45-16:45 Tutorial 2

Power-Aware Testing and Test Strategies for Low Power Devices

P. Girard (LIRMM), N. Nicolici (McMaster Univ.), X. Wen (Kyushu Inst. Tech.)

Summary:
Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability. EDA solutions for considering power during test and design-for-test are also discussed in the last part of the tutorial.

Keyworks:
Power-aware Testing, Power-Constrained Testing, Low Power Design, Power Management, Test Power Issues, Design-for-Test, Scan Testing, Built-In Self-Test, Test Data Compression, ATPG

- Organizing Committee
- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convetion Center, Niigata, Japan

Visa Guide

Please check if you need an entry visa. It depends on your nationality, citizenship, etc. Please ask the nearest Japanese Embassy/Consulate (http://www.mofa.go.jp/about/emb_cons/over/index.html) or please see the web site of The Ministry of Foreign Affairs of Japan: http://www.mofa.go.jp/j_info/visit/visa/index.html. ATS'12 Organizing Committee will provide the visa letters for this international symposium.

Step 1:
Please fill this form (ATS12_visa_request_form.docx) and send us by e-mail as soon as possible.
This information is necessary to make your documents.
We will prepare the necessary documents based on your information, and send them to you.

Step 2:
Please submit the documents to the Japanese Embassy/Consulate (http://www.mofa.go.jp/about/emb_cons/over/index.html).
Then, you will receive the visa.

Notice:
1. Visa letters will be issued only to:
- Speakers / Presenters,
- Committee Members,
- Attendees who have paid their registration fee in full.
(visa application should be submitted after his/her registration and payment process have been completed)

2. If you will be accompanied, please give us the necessary information about them. In general, you can apply for visas together, but in some cases you must apply separately. Please ask the nearest Japanese Embassy/Consulate.

3. Mailing visa documents (Step 1) often takes two or three weeks, and it can take more than one month for your visa application to be processed (Step 2). So, please send the form as soon as possible.

For inquiries, please contact Registration Chair (email: ats12-visa@aries30.cse.kyutech.ac.jp).

- Organizing Committee
- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

Call For Papers ATS’12

The 21st Asian Test Symposium

November 19-22, 2012, Toki Messe Niigata Convention Center, Niigata, Japan

General Chair
K. Hatayama: NAIST

General–Vice Chair
T. Inoue: Hiroshima City U

Program Chair
H. Takahashi: Ehime U

Program–Vice Chair
S. Ohtake: Oita U

Finance Chair
H. Yotsuyanagi: U Tokushima

Local Arrangement Chair
H. Yokoyama: Akita U

Registration Chair
T. Yoneda: NAIST

Publicity Chair
K. Miyase: Kyutech

Publications Chair
M. Arai: Tokyo Metropolitan U

Industry Chair
S. Hamada: Fujitsu Semiconductor
S. Komatsu: U Tokyo

Tutorial Chair
Y. Miura: Tokyo Metropolitan U

Audio Visual Chair
K. Yamazaki: Meiji U

Secretary
H. Ichihara: Hiroshima City U

North American Liaison
N. Nicolici: McMaster U

European Liaison
I. Polian: U Passau

Ex Officio
S. Kajihara: Kyutech

SCOPE

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind.

Major topics include, but are not limited to:

- Automatic Test Pattern Generation (ATPG)
- Analog Test / Mixed-Signal Test
- Boundary Scan Test
- Board and System Test
- Built-In Self-Test
- Design for Testability (DFT)
- Design Verification and Validation
- Defect-Based Testing
- Delay and Performance Test
- Diagnosis and Debug
- Dependable System
- Economics of Test
- Fault Modeling and Simulation
- Fault Tolerance
- High-Speed I/O Test / RF Testing
- Memory Test / FPGA Test
- On-Line Test
- System-on-a-Chip Test
- System-in-package (SiP)/ 3D Test
- Software Testing / Software Design for Testing
- Test Compression
- Temperature/Power-aware Test
- Test Quality
- Yield Analysis and Enhancement

SUBMISSIONS

Regular Session: The ATS’12 Program Committee invites original, unpublished paper submissions for ATS’12. A submission will be considered as evidence that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

Industry Session: This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. Each submission should also include the complete address and designate a contact person and a presenter. Abstract submissions should be emailed to Industry Chair (ats12-industry@aries30.cse.kyutech.ac.jp).

Doctoral Thesis Award: The Award serves the purpose to promote most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology. This major Award is named after Prof. Edward J. McCluskey, a key educator and mentor in the fields of test technology, logic design, and reliability. Call for paper of this award is available on the ATS2012 website (http://aries3a.cse.kyutech.ac.jp/~ats12/).

KEY DATES (Regular Session)

Submission deadline: June 15, 2012
(Submission site has been already closed.)

Notification of acceptance: Aug. 5, 2012
Camera ready manuscript: Aug. 31, 2012

KEY DATES (Industry Session)

Submission deadline: Jul. 19, 2012
Notification of acceptance: Aug. 5, 2012
Camera ready manuscript: Aug. 31, 2012

KEY DATES (Dr. Thesis Award)

Submission deadline: Aug. 20, 2012
Notification of acceptance: Sep. 20, 2012

SPONSORED BY

IEEE Computer Society
Test Technology Technical Council
and Kyushu Institute of Technology

IN COOPERATION WITH

IEICE Information and Systems Society
Technical Committee on Dependable Computing

For general information

General Chair: Kazumi Hatayama
(ats12-gc@aries30.cse.kyutech.ac.jp)

For submission related information

Program Chair: Hiroshi Takahashi
(ats12-pc@aries30.cse.kyutech.ac.jp)

ATS2012 WEBSITE http://aries3a.cse.kyutech.ac.jp/~ats12/

ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convetion Center, Niigata, Japan

Information

- Sponsor
- Scopes
- Submissions
- More Information

Registration

- Registration Procedure
- Accomodation Procedure
- Online Registration

ATS'12 Program

- ATS'12 at a Glance
- Advance Program
- Tutorial

Visa Guide

- Visa Guide

Conference Location

- The Venue

Call for Papers

- PDF

Paper Submission

- Regular Session
- Industry Session

Committees

Regular Session

The ATS'12 Program Committee invites original, unpublished paper submissions for ATS'12. Paper submissions should be complete manuscripts, up to six pages (including figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. An abstract of 50 words or less and 5-10 keywords are also required. All submissions are to be made electronically through the ATS'12 website. Detailed instructions for submissions are to be found at the ATS'12 website. Electronic submissions in PDF files are strongly recommended. A submission will be considered as evidence that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

All submissions are to be made electronically through the WelCoMe system. Detailed instructions for submissions are to be found at the website. Electronic submissions in PDF files are strongly recommended. Please visit the following website for submissions.

http://welcome.molesystems.com/tttc/ATS/2012/

Key Dates (Regular Session)

Submission deadline: ~~May 25, 2012 --> June 10th, 2012~~ --> June 15th, 2012
Notification of acceptance: Aug. 5, 2012
Camera ready copy: Aug. 31, 2012

Industry Session

This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. Each submission should also include the complete address and designate a contact person and a presener. Abstract submissions should be emailed to Industry Chair (ats12-industry@aries30.cse.kyutech.ac.jp).

Key Dates (Industry Session)

Submission deadline: ~~Jul. 5, 2012~~ --> Jul. 19, 2012
Notification of acceptance: Aug. 5, 2012
Camera ready copy: Aug. 31, 2012

- Organizing Committee
- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

ATS'12

The 21st Asian Test Symposium
November 19-22, 2012,Toki Messe Niigata Convetion Center, Niigata, Japan

Information

- Sponsor
- Scopes
- Submissions
- More Information

Registration

- Registration Procedure
- Accomodation Procedure
- Online Registration

ATS'12 Program

- ATS'12 at a Glance
- Advance Program
- Tutorial

Visa Guide

- Visa Guide

Conference Location

- The Venue

Call for Papers

- PDF

Paper Submission

- Regular Session
- Industry Session

Committees

Organizing Committee

- General Chair
  Kazumi Hatayama, Nara Institute of Science and Technology
- General-Vice Chair
  Tomoo Inoue, Hiroshima City University
- Program Chair
  Hiroshi Takahashi, Ehime University
- Program-Vice Chair
  Satoshi Ohtake, Oita University
- Finance Chair
  Hiroyuki Yotsuyanagi, University of Tokushima
- Local Arragement Chair
  Hiroshi Yokoyama, Akita University
- Registration Chair
  Tomokazu Yoneda, Nara Institute of Science and Technology
- Publicity Chair
  Kohei Miyase, Kyushu Institute of Technology
- Publications Chair
  Masayuki Arai, Tokyo Metropolitan University
- Industry Chair
  Shuji Hamada, Fujitsu Semiconductor
  Satoshi Komatsu, University of Tokyo
- Tutorial Chair
  Yukiya Miura, Tokyo Metropolitan University

- Organizing Committee
- Program Committee
- Steering Committee

Related Links

- WRTLT'12
- PRDC'12

- Audio Visual Chair
  Koji Yamazaki, Meiji University

- Secretary
  Hideyuki Ichihara, Hiroshima City University

- North American Liaison
  Nicola Nicolici, McMaster University

- European Liaison
  Ilia Polian, University of Passau

- Ex Officio
  Seiji Kajihara, Kyushu Institute of Technology

Program Committee

- Takashi Aikyo, Semiconductor Technology Academic Research Center (STARC)
- Kenichi Anzo, Toshiba Corporation Semiconductor & Storage Company
- Davide Appello, STMicroelectronics
- Karim Arabi, Qualcomm
- Krishnendu Chakrabarty, Duke University
- Chia-Tso Chao, National Chiao Tung University
- Vivek Chickermane, Cadence Design Systems
- Debesh Kumar Das, Jadavpur University
- Serge Demidenko, RMIT University
- Jennifer Dworak, Brown University
- Stefan Eichenberger, NXP Semiconductors
- Patrick Girard, LIRMM / CNRS
- Dimitris Gizopoulos, University of Athens
- Xinli Gu, Huawei Technologies
- Said Hamdioui, Delft University of Technology
- Kiyoharu Hamaguchi, Shimane University
- Masaki Hashizume, University of Tokushima
- Yoshinobu Higami, Ehime University
- Michael S. Hsiao, Virginia Tech
- Yu Huang, Mentor Graphics
- Michiko Inoue, Nara Institute of Science and Technology
- Sungho Kang, Yonsei University
- Haruo Kobayashi, Gunma University
- Erik Larsson, Lund University
- Kuen-Jong Lee, National Cheng Kung University
- Huawei Li, Institute of Computing Technology, CAS
- Erik Jan Marinissen, IMEC

- Anzhela Matrosova, Tomsk State University
- Teresa McLaurin, ARM
- Cecilia Metra, University of Bologna
- Fidel Muradali, Texas Instruments
- Koji Nakamae, Osaka University
- Yoshiyuki Nakamura, Renesas Electronics Corporation
- Michinobu Nakao, Renesas Electronics Corporation
- Hiroyuki Nakamura, Kawasaki Microelectronics Inc.
- Kazuteru Namba, Chiba University
- Kenzo Okumura, Sharp Corp.
- Chia Yee Ooi, Universiti Teknologi Malaysia
- Alex Orailoglu, University of California, San Diego
- Adam Osseiran, Edith Cowan University
- Sule Ozev, Arizona State University
- Sungju Park, Hanyang University
- Irith Pomeranz, Purdue University
- Rajesh Raina, Freescale
- Srivaths Ravi, Texas Instruments
- Antonio Rubio, Technical University of Catalonia (UPC)
- Masaru Sanada, Kochi University of Technology
- Yasuo Sato, Kyushu Institute of Technology
- Arani Sinha, Intel
- Virendra Singh, Indian Institute of Science
- Peilin Song, IBM
- Chau-Chin Su, National Central University
- Mohammad Tehranipoor, University of Connecticut
- Tatsuhiro Tsuchiya, Osaka University
- Srikanth Venkataraman, Intel
- Andreas Veneris, University of Toronto
- Sying-Jyan Wang, National Chung-Hsing University
- Li-C. Wang, University of California, Santa Barbara
- Xiaoqing Wen, Kyushu Institute of Technology
- Peter Wohl, Synopsys
- Cheng-Wen Wu, National Tsing Hua University
- Hans-Joachim Wunderlich, Universitaet Stuttgart
- Dong Xiang, Tsinghua University
- Qiang Xu, The Chinese University of Hong Kong
- Shiyi Xu, Shanghai University
- Takahiro Yamaguchi, Advantest Laboratories Ltd.
- Masayoshi Yoshimura, Kyushu University
- Danella Zhao, Univ. of Louisiana at Lafayette

Steering Committee

- Chair

  Xiaowei Li, Chinese Academy of Sciences

- Vice-Chairs:

  Masaki Hashizume, University of Tokushima
  Kuen-Jong Lee, National Cheng Kung University

- Members:

  Bhargab Bhattacharya, Indian Statistical Institute
  Krishnendu Chakrabarty, Duke University
  Serge Demidenko, Monash University
  Hideo Fujiwara, Osaka Gakuin University
  Patrick Girard, LIRMM / CNRS
  Shi-yu Huang, National Thing-Hua University
  Tomoo Inoue, Hiroshima City University
  Seiji Kajihara, Kyushu Institute of Technology
  Virendra Singh, Indian Institute of Science
  Chau-Chin Su, National Chiao Tung University
  Hiroshi Takahashi, Ehime University
  Shiyi Xu, Shanghai University
  Dafang Zhang, Hunan University

ATS Doctoral Thesis Award

@ IEEE Asian Test Symposium 2012
Nov. 19 - 22, 2012, Niigata, Japan

Semi-Final of TTTC's E.J.McCluskey Best Doctoral Thesis Award

The Doctoral Student Contest

- The contest is held in two stages: semi-finals and finals
- Asian semi-finals 2012 are held at ATS 2012 in Niigata, Japan
- The industrial jury and the academic jury will determine the winner
- The winner will compete against other regional winners in the finals at ITC 2013
- Both the student and the advisor of the winning work will be recognized

Eligibility

- Doctoral students working on test-related topics are eligible for the Award
- An individual can only participate in the contest once in a lifetime
- Student who graduated in 2012 or will graduate in 2013 are invited
- Participation is encouraged when the thesis is close to completion.
- Submissions to multiple regional sites are prohibited

Submission Instructions

- Contestants must submit a summary of their thesis work (up to 2000 words), beginning with the title of the thesis, the student's name and affiliation, and the expected date of graduation
- One additional page is allowed for figures and references only.
- In addition, please submit an endorsement by the advisor (i.e. a statement that he/she supports the student's participation in the contest with a signature
- The above contents must be included in one PDF file. Please use your first name plus last initial to name the PDF file.
- Contestants are free to submit upto three published papers in PDF version (named: Ref1.pdf, Ref2.pdf, Ref3.pdf), referenced as supporting materials
- All submissions must email to: viren@ee.iitb.ac.in, by September 05, 2012. (Extended)

The Semifinal

- Submissions will undergo a selection process
- Selected contestants, notified by September 20, will be given a short (about 6 minutes) presentation slot in a designated technical session at ATS'12
- The winner selected by the jury will be announced in the Banquet of ATS'12

Further Information

- TTTC: **http://tab.computer.org/tttc/** -> Awards -> Doctoral Thesis ATS'12
- ATS'12: http://aries3a.cse.kyutech.ac.jp/~ats12/
- Organizer: Virendra Singh, viren@ee.iitb.ac.in

PK!   "ｴ[Content_Types].xml ｢(ｴUﾋNﾃ0ｼ#賊(qﾋ!筈Gｨ Dﾃﾞ ｴ盈ﾙﾛﾃﾟ ｳ!ﾛ!嚠暴"Eﾑﾎﾌﾎﾎnﾒ/ｶ*｣5   ｭ/ﾘ8ｱ原J妣ﾆ>f/=
｣Di
dl `   ｵtｶs"ｪ6!cKD   y尻ｨDHｬC_
+♪ﾜ   )ﾀoG｣;.ｭA0c挫   xｪ
庄｢"ｾｱ^   Z4!$ﾇ｢ﾇ}]M1畚ｩ･@ﾎﾗF 肯Qh   ﾊﾊUETI
郛ｵV肘}SC<}�ｬJ捲ｷ､mo㊦2�   fB附ｲｰﾔ.t0tｷuPvﾒ楔ｻn3ﾜi+｡^QIfU^ﾁ同?
ｦｺWDﾀ]9DP   ｽ   ﾔ@l="wlyMｽu�V\<ｨ7@♀iaxﾔﾐF   RXﾔ#rW鉄ｱ@:>ﾀ帷   録ﾊﾒLﾌKｸ假練tｱ�珣ﾒ覦
ZﾇｳYW:ﾞ �/PK!ｷN_rels/.rels ｢(健ﾛJA�ﾟ aﾈ}7ﾛ
"ﾒﾙﾞ H｡w"�wﾌ､ﾚｾｽ｣ ｺPﾛ^踝酔Oｮ寃嶽;ｧ<ｯaYﾕﾘ嫣Gﾟ kxmｷPYﾈ[嘯g
Gﾎｰinoｮ/<藻｡<1ｫ｢箋�$>"f3ｰ｣\�ｾTｺI S書ﾌ   ｫｺｾﾇ   匝ｦﾚY
ig�ｵﾇX6_ｮ]7ﾞ
f�ﾋﾈaoﾙ.b*llﾆr綱),l0ﾏ%搗bｬ
6瀛｢ｴ   _去,   ｡   珂   uZ^tﾙ｢yﾇｯ;!Y,}{清Φ/h>PK!6H鰭 ｾword/_rels/document.xml.rels ｢(ｬﾔ^Nァ   会
@.Uｫ1]z1&ｽ*>ﾀﾃG山ｲ;Uy{'6Pｪ
ｽ�dg˜6ﾛ�
>ﾁｺﾆq07Eｶ�ﾋ^｣i,tkﾀ盈r}ｵy�ruﾓｻｻS｢&堯､ty
掀｡   ilｧ夘[/^ｺｹ瓦ｵｴ"9
%�瓊鰔   ﾋｽMY69<李ﾟ ﾒ坪ﾜPﾛ
H過ﾆ!C<oｸ   p@ﾄﾛuGﾆ,¦Jヴ�擯b竃+GCﾋ/ﾓt�i¦�<鏑,_ﾄQ0EK扱O`≧艪%ﾂｽOBi1Lﾑ簀'ｲｷ淒,!   ｯ入PK!ﾓ!ﾌｯ
word/document.xml�ﾛn8埓_`ﾟ ÅU^｢ﾋ豬¦H0qｯ紊WlﾊHﾜﾛS(4
-ﾇ�%商$收�咸ﾘ7Xﾌﾅ.-畿   L?@ｽﾂ､DΣHY%ﾋNX@wｪ$E"ﾃl   泓   ﾛ斬勞･jｹRBｺ9ｱｦ�wZ兖<¦ﾛ.!ﾇｴﾌｩｶｰLｴ   ;･
o;�¦<兒乳･nｺ^a:'pw鋓ｫ努�八_jNﾙZ&ﾜ硼   s癲   ｻ･ｆｹ_ｽ拗ﾋ墓ｷﾆﾂp滿ｴ*蒜/講Zｺｷ^o糧ﾄｶk趙_97f3c｢?鑰
ﾘqｾfﾟ 2   ;[_ﾀ,ﾓ+�m彁m0ﾅ9}/Cﾔ$暲*ﾎﾗｦｶ�.ｼa?Z   e[ﾝq瀚ﾟ ｻｹ˜cｵ   麾�3孚$K^0ﾗｯﾁﾒ器e``;��ｫ'ｴ
閨,ﾝZﾓ'�O@ｱﾗｧ･JeﾘK�ｽ4F.   况ｿp   zｷｴ;jﾑﾇGﾌﾃ莽#   ｯ{ﾐｧ･   旭n類皚ｶwﾓZｦ�31胡
ﾒﾘXｺﾒﾑｵｵﾔ`ｪ'   譛ｷﾜ;ｿﾐ/ﾔ庘瀅�ﾃﾏ儉>c0s]sﾜｮchﾞ T｢   穽ｮ   ﾜ�究t帋hx舒7X2:x{�｣ﾃ乙ﾒ&
e+[wt滓/uPtﾃﾓDGｻ哂VcRvﾇ7Q#4+ﾇ^!ｭ/ｭ$Hh5l_%3� ┏UｪｻQZBvjﾜｱｦc
q`ｮｶ1ｸﾅﾟ !ｸ蘋4ﾑα   ｣}t枕ﾜ沮Vc
ﾋ   n8!˜囑4X�ｴjaL逸^ｭG�紳"vﾝFｮ�}｢:r:2碌璽ﾙO�茹�止=�斫坡D#ﾞ ⑧ﾑｱ村41\ﾝK5ｷ診�鐔ﾜｶ>ﾅ､ﾇﾌy"ｸ孜

裄Kﾄﾒ｡?i+ﾍDﾋ{˜`ﾘ

<?ﾋD哮8ElE�ｭ8Oﾀﾏ猯3aﾌ&ﾁ堂｡ﾖﾚ=ｸl:5,ﾃF�tmCﾟ �aV目DOn笑�ｩ&ﾁｷ　睾ｭ{,�=_閼ﾐ橦^2(ｸ

?ｷ:ﾒnZj_t　ｿﾛk擦Σ�%<!˜ﾇ蚕",ﾘｱ!b>ｲ7:ｬe�)L'@魁ﾜ殯　　ｦ33　　KxD慮｡P>2r　)rt4話ｮ闍$ﾖｸA0lﾑ紜ﾏ"壽牾

0ｶ5tｭﾟ ﾍﾞe¦Gｽｹz&ﾃ$諛0ﾚt

ｾ4^X升!Sﾏｽzﾔhxｲ冤x糸!^A+ｼCﾒr6　qﾏ4孜　\�夬!工ﾖcﾙ¦mQ7h:店ｯｸｬ"i8tﾀJH}j　｡ｱｵｴｾhｿﾜ｣署G修泙x36ﾆ恊

桧N+ﾍﾖﾞﾗp=ｭｺ唇-ｺ�ｹi-ﾔｻｧ0(　竿ｨ^ｨJE　`]^^(K8　t;�(X愼楸ｯ　ｷ5b\畀�祉z/ﾙ0,　'm+　+7kｷlｬj-ﾆｺ-

ﾓQｯ'賛ﾌ椝ﾋﾚ､�鴨eｾ**:2Z@ﾚL#-ﾛｶr`` -g酌`YV`ﾓ:刄JL ﾑ cF]˜ﾀ?　⑰Y`廛>b�ﾔﾀﾖ誧g･/?ﾃ　｣ｸｺ'czNﾅ

�鋘ｻ1ｦSｴ或�k

;ｦ→8U-｣磔隱{96@｣Fﾔ ﾄd>瘢5ﾏﾓﾍ倭D�ﾒ_ﾆGｯWiT/鰉,禛>ｿ｡ｪ椁ｯ*'(8V)迴高]XV;$ﾁﾀN$1w)1;糧t

1Gｷ熕G;ﾟｺﾐ,l､ｻ!ｱ賤.44lｺ7帝　*+ｱ�{k　;ｬﾘ�Nﾎ,ｷﾔ!　HNｺ�,1�航¦ｹ#b1ｭ篇　¦18Aｼﾀ2p9+;L9OKﾐT@NK?

@ﾐ桑Pﾇp魘4ｬｴｪﾔ"�h冨#ﾛ噐S"tK,0ﾗ0=横Fjhｷﾃ E5ﾉ)ﾙｷｯi]r　　^ｩ/ｯﾗ5ﾏk'F(ﾅｻl(ｹﾞ)ﾔ]z鬲ｆｳｴ誧R��f6�t3　r

巳'ﾉﾍ逾〇rG2sG�　ﾐｹ　ｨ<>ｽ蕃1ｭPﾌjｯ｣-笛&帳n7�ｶ0浙-愍ｻ0Dg釋胱懍fEﾇ

`$'磋勧嬾 ｲﾑｹp.yﾈﾛ膳xuq&ﾄﾈて9=+ﾓ)yng　　iｩy.ﾄl#醯ｩ偆�5ｺB5紂t�r+ﾈ+j姻&♂�>､ｲﾃXlﾜg薄Hvﾏﾅﾎ屆ｷｩ

ｽ09ｧTM�"逡:�F�胚Wｿ空　p^V*ｪﾘ　ﾀ｢@Q�/L˜　j+　俑,｣ｽﾞ#"ﾃ　.G�s6]///

$ﾐZu5　d/Z　ﾒ9ﾆW_ﾂWqｸj*ｺﾖｸﾗjﾔ<鑽py6ｸｾy>瓦mkｽﾙﾅeｭ4ケ纛Z

\q]ﾂ諶｣ｿｻﾖ

^kﾘﾀ+HC(�｡;Wﾁ;ﾓ獻eﾍｵq7wﾏ｡ｵﾞﾋHbCﾂ#ﾜ梶zxｹ*a構r随aｲD　$¦%aDd{pｻﾖｬUｩ/{&&唆;｣+ｩ　X%虔�ｼｺ卲玉

m莖t"｡　jﾞlﾟz ﾃA薯G{)ﾇaﾑzpﾜ;2Йfwﾘｱ'ｩ椭xﾏk˜ﾊ�`ﾛ　ｿ　珸eﾖ

b鑒ｸｻ;恂ﾚGｾ蘖ｨﾁ?˜滞l%　HV3ﾁｩ4.Aｶ Ty0ｦﾞJﾖ zEY]ｿcﾗ�樋ﾊ%辭　#砥&　Td"ｫ Z8　C

�ｴ3械ﾅg　ﾜ8　　　ｩ%R那l%C%aMXJｾ捏;m資pカNﾆDlvﾖ2uGヌt=ﾎKD}""' #45�ｺp焔?1ｮ^!ﾄ{8Oｷ｣P蹌z^ｯ

cﾂkH｣ﾌaｱ-ｬ照ﾄｬ4ｼ

"ﾛ:ﾁ朽Sｼﾝ顔>_秋悃ﾇ　d濮iｬ˜E=i"sﾑ々pD盡@tDb咤.執 曩ﾈL�R　7ieEX｡{�fﾎｮlｨ

ｿ7U､ﾙeｺ{ｻｵ>C萬#[ﾑ!ﾞ07ﾓmｲ桃lR¦胥�b<ﾜ亨　　lsd9oY祈K}Dd?-3yﾔｫ7祝ﾙ ^ 疳Ⅷ

<侔ﾁ0　GN�1殿旛l6擦%E^�!5<GVY｣l\}

{B剋ｴ;ﾌﾖｵ/bｿﾎ1､˜ｮ7N1�覊ｷNYｬ<m　�G,4e>F･ﾈｭa｣ｺ�ｩB�/ｦdﾞﾄ6.a6vw+ｼq?l　dｿﾗ朂m.8\&｢ｪ-ｯ<南

x,y�　　L譁;　ｶ1v!f誌*哉ｿ　8,%�%ｉX執Ds濆K{=ﾚ��QTタﾘQ�.Y¦　飄N寇覦>)SG応lｬﾇOｪV･;Nｦ榜sｲba-

¦�ｿt@ﾌ/巽7ｮｭ�菽T¦$�<Y閻檀dﾁ$ﾔｳｦ-y､\擔ｦx戦　%d　[ｵVｩ

@6罐 料ｩG:噬9恵w@ﾐﾃ,釭ｽﾈ;ｱカ套`1

ｸ0皇XyR("

uｿVｯﾖ�ﾄﾞ!剃_*ﾆG}ｯ>W淀+�d3ﾍｺ%ﾙｵｹ　q$ﾚｵｹ=@efnp豎L7N¦　V)F-_kV壥晴q2｡¦=氤]　-SBwﾗnﾕﾎ手ﾈ仇,;ﾕ羽ｼｹ}ｸo　　ｳ4跣?ｱuBb如[ﾓ#B%ﾎw˜qﾄﾀ)(R絹ﾎ}　U¦ﾖy垓ﾋ･D旃ﾖｻ頙ﾌs¦ﾟKGXQ競8ｸoP\ﾏ･_!X*�　z秘

ﾑﾓ　;">%ﾄnﾈ鷺Tｵ)?ｯ�7儒E3ypﾜGk

{L諛ｿ働ﾋ[ｵｺ?6ﾍ･ﾇﾝ!C　J,　Kk^,艮@｣}Lsﾍｼﾂ鵬ﾚﾞ#Exｴﾙﾎt　WB弥

見ｱC@$ｸwｪﾕt>>ｿ\wｯ?E鎧1lﾘjﾝzｭ%>1'q　-*�!ｵ勉H狄a妤(ﾊGVﾟ晥｡ｳVoｭ朧濱ﾌﾎ:D俺　ﾔ?5fOdG>　　C6Nﾓ-

9　ﾐ0- 2粉ﾋ･>�gZ:欽\y罹f｡#ﾟxr(ﾖfﾆb@&ﾊ恍ﾖｷ6LU霈莪ｳﾛﾐﾎ$2�ﾁﾁｷ@RFﾂﾖg_ﾐｯr3ﾌ　ﾊqｴｲH｡,ﾘ"ｧ

6ｱlXｼ　ﾍY.ﾊﾆﾁO軈ｷ8Xｭfｦ圸k%$ﾎYｷﾞ{Q:xﾄ\d医7扨Ggﾝ C]ﾐpﾛL=ﾓ　5q"%(*Oﾆｭﾞz+ｼ9｡禁4\瑙ｻ　3H(¦0煖v

ﾖﾃ/框ｪｬLﾔﾀｯuTﾘ檸ﾞ悶IDQf_H=�$9　6 ｭn糠D､3呱ﾓX,¦.ｹｭO{gﾒCﾊ�>ﾇｽFwﾀ　　�ﾙ�j,Zc鋐kｵJ杆@D*PX

史ｽ缺Pﾜﾃ*3y銡2W$ﾑｯﾀ　　告&˜

ﾍJKd6踄n掲ｪﾈ睛ｾｷ=]>_AY"醪6>8　ﾄL闕(s簸ﾖb｡#ｿyhoﾌZ-$os-

椌DWV3ﾛ蒻ﾅﾟ!.h�題Uｹ8ｭ晗效rb�H;]ﾛ6`ﾑMPgX　霻h,絳,早ﾇYｵ　-ﾚ/a]jyﾌｵ3ｴｭ禅@onQﾟl;%X　ｴｬ単jlｦ　頓癧_ﾟ蠕,tnZﾇｵv-辭ｿC狠ｿｴB

mM/ﾂCH廏sｱｯｯ4ﾛｽ-d　ﾏ+　ﾅl@)SVHｬ9¦刕ｭ飛wｲﾕ｡ﾃ良ﾃｶH懐;d(%F宴65ﾛ

Q:+ｩ肬ﾇJ^�$ﾙﾎ'FｺmXS\ﾏ%　ｱﾞ閤�　Nｧ　tpD咤<ｩG繿-4ﾛｬl7鼾A稔∮ﾓﾖYs/r呉　%/ｲ˜ﾚ'

蹈0yｹ攀ZG7˜萌<ﾘ　ﾓJ衾*｣ｪﾃ2ﾆ}M]N�閂ﾐとT粃�Jl庭8ｾﾝ=ﾇ温/q逃m号;華ｺM菜ﾖ^　裝ﾂﾀ釆ﾀx�Rｯｭ

ﾀﾓdｸｿﾈRe鶻:iｱﾔ　Q�nｦT哨　HJ扣肯?ｭ誧=ｨ=

�ﾎ@ｼ蝋2@j

#glﾁta

犢.ﾒ飽從Hｩ壁L8rｿl/`^i+ﾖ;H縒QLBﾊ　R(eﾕﾈl堕　^#D�俟B奘坏A}ﾝ打"惟ﾃﾇ嶋?%匂觀#寔ｲLnrﾄCBiｩ6殊

gﾇ｢%/G[�匱匸kｳ　o虞涎　�3ｯo諍髯ｷ　ﾚ峙⊥鰾｣eｱﾞ位D7Rﾅ　･+g　u(�l<　　褻G&ﾟ"ﾗ舵.　aMﾁ･a嗣?癇ﾟﾐｲu耒DﾝﾙLロaﾇ　ﾜ6^#1�tu葆ﾟ.

ihｪｻ-,惶CｻR　渡U\6 y

1d諡{　鰥ｺ\將G5+^F6K管ｱﾖ｣?i+ﾍ,冒HhS鈍振�<ｱ膜ｿ｣-/Xじ]髀ﾈ;3､k:ﾆii,ｸc于.ｺﾅﾝｮchｸﾝ橾蒟`SwｵZｲ(z4牀ｯ

{ﾍ-Xｨ蒻　wﾇpｬEﾚd｢ｯ@z｡4　赳ﾒﾈﾟyYﾒHl矗.-ﾀ?ｯ˜ｻｸq:/稱mO亭獺#66靃

ｧﾅgﾗ{ｷ墟_蓮uUｷﾗｿtNI�{[ｭﾃRｩ　N　^¦｡←�ｿuf�Oﾗ/ｸ-ｬ/　母竑ﾋ;ﾛ倪lﾜﾁﾏ楫ｧ痣ﾏKﾟｹﾋGﾇ5ｲ!　ｭ}ｪ2@x3}｡

kﾃｻﾖKZθ`@趾　ｳ&ｳﾍﾊﾘﾆﾍ籍ﾕｷh"朗oﾑTﾗ<<　0　M豌ｦ軌2�N催�　p;˜6Dｸ晶降ﾓ[t艸;｢aEbA康K�}ｿﾞｿ橢ｯｿ肭osl\H1

覈q豢=HAz教7ｪ[雛･fｹq｡y6ｦｾﾈ壗D　鉀陽ｽﾒｮU峅ｾ楯g^dﾏ�$ﾃﾙﾃ　+\#ゃ/善嚠+i*ｺHa"4e!統

Xﾆ1�]8ﾜﾖlｾKｿX>　0N　ﾞS瑙L(恒v殃a憩ｬU*l枥/ｼ9Nｽ]麦a.ｸipｲ!

ｯ捜˜75纖納e

ｷﾁ](ﾌ ﾋ鏤 蚌8ﾓ湟]j琅+」棘Q鵺ｨﾒﾝAWkﾄﾏ(ﾀ]啌掠sTF葳>ﾑﾙ =GﾑｨdK� bｧ8斟Y

&9惰�(ｳﾛyﾒ5;ﾎ%'V�ﾆ2､tﾂｴGﾘ�:ﾏs!N˜=釟rﾒ獸T{ﾊ4ﾛp+8 xｩ

�!ﾔｽ-tV縢､ 柎W;Oｶﾃﾉ NpJ誤舗胝ｩ豈$懋4ﾊPcｸ鷺恂?2ｦ 袱ﾟｯｷ 媚 ﾗ示神Dﾈ A鰕間ﾛ勅UFﾗB陋 #4ｺ」ﾑﾅyｯ

{5˜煩

ﾘｼZO_ｴ @Uﾞﾁﾄ3凩q蠖ｦ*��岡W疆CSZ坊庖ﾈUyﾇ]ｩ閲腰脂}"5A憑Q婦sﾝﾙN ﾁT蝮sﾅ6 ｫｱｪ悍鮠V庖

WﾄkUy7'ﾏ芒Uyﾇ販ｲ活T=[zｪﾊｻ+$ｹｫﾊｻ｡mjG備�](*ｴ}ｩﾊ;轍4Uy龍+wN梛BAeｷn9dﾚｵO-ｴｺｽ%S8Uy掠彌繩

ｴ!ｪ u8･*�}梛$

H盪ｪﾊ鮫H拈蝮ﾟw�蓊��罨ｱ2抱貰ｽ308� ﾂFﾔｮｯ uUﾅWU�'LXIﾄﾞｮZ?�˜ﾎqﾟUﾅ樵¦C烋]ｵ˜枉u ｹｭｪ ｨ

ｨｵﾖﾏｯWSｾtｽｾTU�ﾓNb鬱U 燔Y罌ｪ祠 PJV膕U¦Uﾅﾟ US蹄TfT�｡δKﾊc湍･ﾖﾏ31益ｿTｿﾀ*�Qo0+戻嵐」

ﾍ)KPﾂ ｹ烙%ﾀﾈv啼ｿﾞ>]啼ｫﾚuoﾍﾓ ¦ 輛 ﾂ**ﾑﾐ�､ﾆWﾁﾇ'�@J洲犹:x"Q閔Uzｲ!) #ｨ､竅簔C瀬ﾚLﾈ3ﾉﾝ1邨

勅")ｻﾐRG寛芦Z ｩBﾉﾈｳ ｻﾇﾟ9"ﾝFH ﾄb當ﾋrg;

ﾖvｴﾗﾃ¦宍(4圻:7=&@dﾛNx籥uMwd_�ﾏ# ﾋ鰲ﾗ)qﾗ潼(7睛:ｴ

毒z./7=> /TOhE_cC 仞{ｧ鞋ｩﾐ詛i萎ﾞ.b涜QﾇﾋEｮ7eｾ]{/Z2ﾗﾎﾔqmｳ#ｻ勝ｭ;付ｧ｢鱚ﾎ6x vA龕ｺy伜X'>-ｧ

ﾝｵ!)h･u･b5ｷ .ｿGｺ･�ｴR5<分˜a VﾒTﾅB

8Y｡ｽ?[} Rﾝ 2ｵD膽ﾇe8ｳ&ｶﾞｮ昴5}o ﾇ6ｺRｼ譁 ﾗｹ･ｯ播T渠｡�sﾇﾙﾌP晢9Zmｻ迫ﾀ@ｧﾈ綫Goﾆﾓﾏつcｩc」)-YM%T#f*-

¦lOL

^PK参�今++Zｵ'PK!�sUtﾟword/footnotes.xmlｬ塚n0E ﾈ{b脱ﾒ｢@､ｱｮ汯ﾗ倭{,ﾛ@ ﾐWEU7Fﾌxﾎｽ纖濵]ｭA+ｬ蕩

ｲ\D$咤!>!/ﾏyxC逋.X

Z$ ﾙ･ﾗWﾛ..ｼﾍ滓ﾓ庖&ｦﾔ (`�d V1樵vOｳo 9(ﾃｼ¦雰ｺ瓦51瑞ﾆ黜DЙrJﾟ瞭P亦虞3UﾘKt助

EjE@ｻJ7ﾑﾔ_iﾘb5AﾚsMIｴ榀uｵﾂｨ｢凜la,pFｳcr&.」sﾚ ｹﾟ5''蟹=c氿1yx=jﾓ ｾE鋹凾.$'ｳﾌ%脱Bﾂ蚪

ﾑ/nk (ｺｽ[m6Yce｢dMgVll˜ｿﾎ ｱｽ莅@ﾓ-Eﾂp壯弖諢3ﾚKﾝ并 e &O茅3拳L硎PK!@!¦uﾙword/endnotes.xmlｬ溺

n0�布=1/"iQ R宜W9kL-=ﾄｹ}Dm」(ｴｺ1 轆o�ｻ焄uﾐ

$闕, �PHｽOﾈﾛkﾞ訖yｦV 9Gv鳫ﾍｶ球.4xDhｷ事ｼ71･燦B1ｷ#4&K-楽ﾜﾚ=Uﾌﾞ4&茴]ﾖﾒ*関dﾄ@Bｫ*ﾉ-

8(}_CYJ.ﾆﾏTaｯﾑ=Vfﾀ%ｴｩ5z*iﾜDS･a琴i/5ﾑｴz:ﾗｰﾔ

ﾋ:¦Umw`c03q]ﾒ/-Gﾌﾗ X 99QLﾓOﾇ譲o￥G詳ｴGﾁｻHOｳtｧ?9a脇,ﾁ,.kgｷ8ｫﾅsB｢aｵﾙd!秤5ｵ掣鶍 :ﾏWﾄ ｳMｷ

ﾃj��ｾ8h/u3枯ﾋO肖?[<+vﾁ.ｶ1馴PK!{oRword/theme/theme1.xml�MoEｾ#F{oc'vGuｴﾘｱhﾓFｱ[ﾔ繆wｼ;ﾍ�jf慟

7ﾔH\瑞qTj%.祢ﾒJHｼ3ｳｻﾞ荷JR"ｨ>$ﾞﾙgﾞ�_ｽ f閨lyﾒ 槵"珂噪m�-iﾍCR$ﾀﾞ､仡廻ｮmｼ鮫Uｼｮ"ｹ杓ﾍ､Tｺｾｴ

� �

$}Xﾆ2OI \ﾄXﾁ」] ﾌ末kｵﾕ･ﾓﾄC 氏 }t¦ ko#gﾐcﾀ%QR/ 4y粮2ﾘ`ｿｮr*ｻLﾌﾚ

<PbX*xﾑ 跂-m\]ﾂ�&ｦ-湃娑ｶ/ﾛ/"LF�VAﾟ�ﾇ ｽnｯ^ﾐ3�ｩ払Lｳﾑ_ｫwr%:Oｻ[kﾖ.ｾDeN觀ｧ

ﾓiｶ2Y,Qｨ_s ﾚjcsﾙﾁ税7銜歳ｆｷｻ�

ﾈ禪銜+ｭﾕ�7尉dｭﾚ�ﾔﾈｰ舁ﾀﾗj¦�h(｢Kｩ -慣ﾟ遖

dXﾑｩiﾉﾆﾘ⑨ﾞ3Mｯ\Zｷkｾ弾ﾒ恊MUﾛ{?ﾅ3jｯ�St�ﾙ 沁庶h 9ｻｶq殆ｽ�ﾓ?x教ﾋG欷綟 gｺ@H棘8/ｾx ｳ'/

ｾ� Uﾀ7甫C頴ｸｷｴﾇcPﾌXﾅ復呼 #Lﾋ;6撤k. *rﾐｷｦ倔

\�ｼ+xTｯO;"1Qｴﾔ(v;惶彪ｸ｡y蔑<$a5s1)膀0>ｨ籖ﾅ峨ﾟﾞ$�Iｫ Hv#ｴﾃｹﾋp｢pH｢厨ﾇ ｩﾐ･讃wｨ/ｸ臘�Qﾔﾁｴﾒ

$C:r｢iｶi嵌燉i斧灑ﾇ6;wQ�*ｭｷﾈﾟ ┏ﾈSﾑ ｺ!aｯ繪ﾂq/!産ﾙ7ｱ巻L�ﾆ OTEﾚqﾔ�U{nﾐｷ蔬鶫･ﾛwﾘ4v腺ﾑ*71

軻ﾟ�8Nｫ-咼e�rB」]ｮｴ;ﾜﾍ~ﾀ/Bwﾟ･ﾄq ｺ

素｢ﾟLD(ﾔN絞ｲｸw｡櫻ﾄﾔ 苗(/ｾz\oj!.5%'ｶO悲Eｸ摘ｷﾋE@ﾟ�ｻﾞ/.0殪<oK飼庭蹶鈬¦>k｡旌V(ｻｺrﾘ滞ﾈ Lｨ)#7･

% 吸9停ｼ認5ｫ.ﾘ�きｨNaｼｮ{唏(3ﾒ｡D)用ｬ3ﾋ紛5Fte�}\- bｵﾃｻｼ｢烈SAAﾆt嶢=sF+埖Y勵\/�ﾚｯﾃｬｮ:3ｷｺﾍ:Ⅷ｡

2 ^5X,ｬ こｬｼ

'tﾍ&�@ﾛﾝ ﾜ-ﾆ"痼d>ﾒzﾏ諟n恃ﾇ柑ﾘｩ >笶bｵｷ&7ｸ敘Iev�/< ﾎﾛ鯤池rｲｶｽVsｹ!ｧmo'Zｧ炒ｩg>ﾌBｸ -aj2,毓ｳ

+&A.)ｬﾝv鵝*､ﾚﾂ2ｨ｡a^e!ﾀﾍ/ﾊｿﾜｳ^6ﾒ_C兜5M

-」�2_幅]Zﾑｶｳｲ什)Eﾄ

ﾑ�ﾄ P}*疔ﾂTｷhﾚﾚ謨[惶､+ﾟ]彎ﾇ,膏Vnu頑冤&ﾌSI<ﾐｭRv」ﾜ 1)Aｴ氾ｦ基'pS-h +0ﾒ P*認ﾔL塚h○Xx

Aﾗ/豼 愱ﾍ9Kﾃ､5

蔵ﾐ週$ﾙ�d｢b wY,#d"ｪ$ｮLｭﾘ#r@ﾘPﾗﾀUﾝﾛ=Aｨ鬭潴;罇泡」P9蛞sjHﾑ{m�楝MfPﾊｭﾃf/慊�ﾑU埓ｳ=�eE ﾙ俔

ﾈｳ�ZA+K鍹癧ｭﾖVｬ9漉峪p絛y溝ｱ�ｸ�?*¦FL�:艪P[�陰ﾘ@T_ｲﾒﾒ.餮pｲ64)kﾚItﾒVﾋ麼Oｺﾟﾆﾖ喋ﾅﾟ4v1

惚�\ｼHcgvImﾗ<{2Eaid慶ﾌ住袙戉>8zn'LIL 賃0zL@ 伺�_PK!e-6ceyword/settings.xmlﾄWKsﾛ6ｾwｦAﾃsdﾔ

Xﾎ '羔(iﾏ I栗B豬_ﾟ大ｬ3競zｱﾁ]�ﾛ S]ﾍ蚕v･hV�c3ﾞ兹(巛ﾊ 9廐ﾆｬSｬ)X%ｾ2ﾎｼ3ﾞﾞﾛ)離R-ｭ宦協ﾄﾊ8ﾈ&頸=ｯ

Y7ｯﾋ\劾Iｺ<u ｶﾛ2釟?cI+cｯT,」ﾑ紘yﾞｶBﾖLu7Bテ" ﾍｵ-Mﾓ[H^1 w軏&o｡ 薤ﾏ8ﾖｺI�?ﾛ9本ｲ +駟ｼ栢w

[WCｹ5+嵋MW粥ﾏmg#<?srm&D=;-9

=7Mc｡ｷ?�､�ｸdｯｪ3!ﾔｨ. * mﾖJI猜 Uﾟeﾗ V�/d 4涯嬰'ｨY)ﾌﾟyｲｸﾞ7略ﾌ_ﾟmｩ轆&Yｩｬ[麻ﾗBHQM>a[

�<4ｹ: 3ﾘｹﾞｳ'C ﾝｭ:-ｫ馭ﾇ?Hｼ(┳,j 2霧wｷﾇ@」#枅eｧae浙�

?ﾏﾖ:ﾘ竇g頗韓-`ﾚｬ･nﾊ･版ﾊ麓C/ﾄ=h灑ｶｼ).屡~ｮ･筒+C

S:ﾀ蝎神�`krｾｼ+Oﾄa3ｬ)ｵ7z8; 蜿]ﾅｺ}ｨo耽yｨ>KVVｺi Bﾟ>ｵpﾟｬ V}

赶~/+ｾ: 6�僚ｽzﾗﾀｨU」沁g;泣たﾃ%gｸﾘ

h)ﾐ軌4ｦ ﾛ ^枕､ｵ絞:4ﾍ､_jHD<TCﾌ鞍ｨﾆｳ泳"'ｴﾐ8qｵｱ<ｺI)

ｮﾆx洩<ﾓﾔ&tIJPM鶻ﾍﾀNiどqｦ!賚qm+C+uBｻhｮｮoｺﾋqﾞｯｻ猗守｢捏休hﾄ｣$BmHIZ痊俸ﾇ　k癜R

孵:ﾔ　叔}　CX(:4u　　對､)ﾚ9噐I��ｶ劼s　2C脛ﾄ!xO}浪'ﾂrB_/ ｣~譁ｮI麥鱠0L-8ﾋﾈｦﾗﾄ0穏ｷ六&ﾚｹejﾜh'恃

ﾂﾂ4!qI=%大AE弄�j"�ﾜb釧　ﾚﾓ8麻ﾎN���ﾋB'4v�ﾇ&ﾁ�S3ﾄg4ｱﾋFｱN\B"　q}訌t�ﾎhBｽﾄEｻ拭bﾜ&ﾜﾐﾛ

%u喆c]H=s鬘始KJBmbｴﾛ'ﾅ s0Aｱﾎｴﾒﾌ'刄榠ﾗﾍｲ漏ﾚﾇ＼F

6ｮ′ ｽ&ｵﾓﾔ8[ﾌ鼾,ﾙ�貲　Z箆､ﾟp琣�ﬁﾘLﾊ　Pt5ｫｪHﾙ､J<h4ｾｺ;ｮ>0ｹｻx/:勢(ﾙ靃ﾞ4u褪爲浯$Y頼)@<ｴﾜ＋

ｮAﾙｫｨ'ywﾘｬ'ｵ頌3ﾕ｡):J厓q(xﾑ/ｬﾙM,7/kｾ8�ﾘ浜e¦e　ｵ5辱ｮ　`m　　　vｮﾊｨ4uｱｴ函ｯにﾇcｳｳG昊�K�耶ba　ﾐ

%3/恚ﾌ拇珉F&ｹﾈｼI詈ﾙO━I眞1-ｵ¦+ｪJ忸q? Wﾆ｢�I/ﾔz蔕　Jxﾅ5ﾃﾗ$ｾｽ槻

ｦ;　ｸｧ/

9ﾏK　ｹﾞ\^7CｺUﾙｩ5o瓣｢ｼ倞ﾐｰｨ.o貊PK!Jﾘ樺ｻword/webSettings.xmlI湖ﾁjﾃ0ﾆ　at_暄0JHR(｣/ﾐ\Giｱd$mﾞ　5I

累z滲　_im>Q42

m｡A

<Eｺ

py?=�Q4　　　　　�　飫W　Fｳ寘MUH;`1ﾋ捏L^ｷ恆6ｳ$o　帙yﾟ8¦$$sｻｶ}uきｷZKﾌ

ZyD+,SｨZCﾒ桀%　ﾆﾚﾈﾙb?xb9

Eqcｵ舜PK!｡ﾃﾈ　xDword/styles.xmI�^rﾛFｾｧjﾟ�錝EJ被

擺h+vﾊq奈=CﾀPDbｴ,涕V�rﾋﾏ!9橾U0ｪ5ｯｰ==!D7W侔$q0ﾓ_Owﾏﾗﾐi毳v9oD中2ｹ�　Gﾄｾﾂ　萓棍ｿｻ:i貲/X五

村?昞'歉?Lｳ姨､意�ﾈ挌ﾙ　ﾁA�ﾅﾂK?必ﾃｳ儉^突9寉ｾx"ﾕBﾄﾙAｿﾗ$"2O蚚2u唆k感kﾋD"MAﾛE､-ｼ0v】♪汕匚幹

T}Lﾎ　¦ﾂg2ﾎR鋺｡簾a8ﾅa給0緬ｳﾇqｺ　xi8

ｽ�god ｧfL=洵嫁�･歿〒aｺ

$1,¦紘#ｷｯ�wv0+ｽ$3+　ﾋ¦Lﾄ　O期剤oｽ{_椨｡ｹ^ro　;ﾀﾍ?FXZ梢Y%求_ﾀKｸ合-ｧ仗&<ｹ)8　　ﾊ$ﾌnF蘿fp"盖0

ｪ¦b<　ｹ�ｧ"Xs!b$侔g`倔　z1J｜o}ｱT!xｱｧ<　-�ﾘｴ

ｭﾂｵ6zｍ�蜷ﾆﾚ[Q厪Sﾇﾀ Aw皸Wｪ�jGﾅ

\粍�"尺8n/bﾘ^ﾄI{@~m=｢c｣付ｧfﾒﾗﾁW潔ﾁM[CVｭｨDQ縄Jﾐ4ｮｨﾄH縄JH4ｮｨD@縄甘WT�ｸ｢箕+¦沖EI饒

Oﾃ,jN:IIu&)8鮝秕&ﾞr鉦ﾄXV{YNVMU､ﾓ/r%2ｾIｴH_�9　b9　*ﾓ　嘸鶵Dﾂ"　　ｪｨ$,*ｶﾒﾁy蕀b.｣@$ﾎTｼｺｭヽ~K餃

満I-Qｷ某}^ﾎ3g2ﾇ鼓6d[Bﾋｦh�giXｳ布3i$kﾂｨ^　"W衿4�dｨ鬆礦ｪｸﾛDGﾊEｺ3ﾜｸﾊｾｶ濔　ｹ/_　｢ｿﾎD{ﾊ'隸　橙

1>v煇g9�'^r蜷邪 隲仔$逭*ﾊﾏ@#=慍O-�m土渥¦I慍O}:殉ｾｸQ笏宊52Pﾘ皦*�2-ﾘ*aX昤ﾄ&ｼW崇ｨ

nﾄMﾈﾒｶﾔI<ﾎ@

"片ﾟｬdｮ\B　8所<�巳ﾂ｡｡

jNﾍﾄ鳶wｷK¦vﾔ.2j銮ｾ曁9ﾒ>92-ﾘｴIｳ9ﾋ慍叨aｽEbﾓ　ｼIｨｿjNo},T&�jﾞ$-ｽSﾊe6o-ﾘ*aﾙｼIﾀｪ/>*r*gS�Y粮ｨ&舒

&uCﾞ ﾝﾒy-ﾘﾜ`9ｵHﾞ 慊 o♀膞bsﾃV)ｻｿﾜv@ﾞｶM膞@a{ｧDｨ也X8 %,Kuｬnﾈﾔ

yｺ!oP7膞黽ｼ @栁ｻ､;&`ｱｹﾁrj他 @lz-@E&7l%o<攵 (lU/它ﾂ 乢ﾖ-y-ﾘ*aY&`N0,nﾎｦｺ!oﾂ室!oP7膞黽ｼ

@栁ｻ､;&`ｱｹﾁrj他 @lz-@E&ｱｹa+y綢�膞@a;ｲJﾞｶwJ�y死ﾅvP ﾋ7罕5ypﾊｾ@uCﾞuCﾞnﾈﾔ楙妁ｺ#o,ｧﾉﾄｦT$oｶ7梠

蒐ﾞｶM膞@a{ｧDｨ名 Xl焚,ﾕｰｺ!ofk&癆=qﾜﾔ

yvﾔ

yﾚ努3Hw膞ﾀbs�ﾔ"yﾘ ♀膞bs�fﾗE/ｷSk�zﾏ ｿｭ@�8

h6 ﾌD工｢ HKﾀ¦ﾄ夸n ﾊ+�ｯ{P dｨ"

%ﾞ霎ﾁ[:>�/薩るﾗc逋ｩｬﾃ接ｼy-Fﾅn!ｭ蜆ﾝagvｩ ь 抛˜ｱ\lク"ｺ貌:p穐 瓲u l¦2}>/[袷Cｷz積鵶ﾎﾆﾃｳ3ﾓ"-M

:蔟ｮｰ'2ｲ ｿ 厦M悩=bｺｮｰ;�tｫ

�ロヷﾟ 9˜ ﾃｯTｻｯF-宰˜:rｧz膺殼逡\xｱﾖ!}Wh鶴怪ｨZﾐ气 L$ｻ,ﾘｫ于詛?嘔ﾝV兆$o>ｳ]Uzﾞﾆ EPｪ

ﾗ2Sｷﾙwix XﾑP;ﾙﾁ{ <Uｽｯ5YWｨﾛｳ7ﾂ vi�/ﾏc1ﾐWﾓAｼ Xx>Q �ﾏ莫˜j$f凭zﾘﾃL^A碧E/ｺ｣&ﾛe玉闖j&集

遭;倢Gｫｿﾅ�ｾﾖ6､ﾐｭ糢zm !T4Q}vﾖｨﾈｭ＼ﾛ 罅(険rﾅｼ｣ ﾒﾈﾆﾘ4

?s\u･Vｾ･ｒ}ﾔ?6粘�ﾎUﾑ輯 W藍#/鎖薺b疏�]ｴｵｻ4g｢箪v}ｩｬ�^9ｬ萏R泳ｭp炅ﾅ咢ｷｿﾜﾝﾞﾞﾝviiiｽ ?}瀹

˜ﾋ(@#A)�u>g e'3 L<djｾ 終ﾝf ﾀﾊﾊ 鷩ｻﾛU聲13黥ﾎﾞﾝX]ｬｳ ﾑiii&ｮｦfｸ搓 � 蓚澼ﾏ2b6Vｹte困ﾓ詰

52rm-b〃Ms､ｬ!�ﾜ4]7ﾘmﾝ乘y6^{z:<�二tｯ)黍0¦Yxｵｩ+<ｱ WKｧ xg━Ruｵ5ホ

�ﾇ;pｩJ)ｴ跣

 毘ｫL鸛0ｵﾔ^km攘ﾗ�

ﾛkq/¦ﾄｳｼ0瑁Z/�ﾋ,@}X4S髫滉 PK!鑁Tﾒﾘｪ

word/numbering.xmlﾌWﾋnﾔ0ﾝ#濁m馳7jｦ﨣JEP!4扱' ,�l',=.`ﾛ˜Oｷｮ的ｪ:ｨﾙL&ｾ>¦¦瞬sxtﾅ剴･ｩ! =/�y萎

Mﾎ ﾈﾑ3)HD｣｣ g⑥ 2>%

ﾄ:ﾈﾁｮｫ｣aｬ JgRql澡^]遮,ﾝ$Oｱ｡Sﾊｲ YｸﾏeｰL荏b蒋Hl-gﾆｺr6｣Y>j ｼ慕荊2N)3ｺ0ｨA

斷Tﾗﾑ ｣ﾁ:H˜ﾟ&rﾎj\>$[ｬp<sV評HｧJFDkX=ｫ勲Dﾟｻ/ @｢ H 9�8ｦ｢ cﾛc腋崚ﾛ�sｵﾜｮ

 #ﾀﾅ OｵQ82wﾖﾞ.y%Dh-ﾇ,Dﾁ/駅 lX�3f+6Y､､ﾆ$叫｢ kcﾖVa

OY昨O訶Sｯ{ZYXn

6#5) ﾕﾐ向aUHA卮ﾝｫA郛Y拉ﾓ�性ﾆt {ｳ2ｪﾃ02[ﾂﾓ7ﾊn

ｻOｻｨﾘZ,譏&ｻ2ｫ[KIｪ慟ｹF�ﾒｽｴU1 ｬ^ｱｦ8Dw7?絜˜9ｷﾗ_nｿﾞ+ｯ ﾄﾞｯB9ﾑﾎ%)惺団8eｨ

ｨ(&3憇后evxkｶ }�q頷ｼﾏ ﾊｲﾎﾞ˜yｮ�珵鱸�)誇)味Aiﾞv$ｨｳEﾐﾙ 勒ﾏ] �= uｷｪz�vﾐ鈇�｡cｬ jQ>Aｽ-ぼ!

ｱﾎAｯ j�ｺoCﾁﾘｵqlｷCbﾝaK.鰾A峃\9湜 ﾘ防vHｬ7xｲK譯冨ﾖﾎE0"K ﾇﾙj�A\ﾘｯｯ很�仙

xﾏkPK!N$錂xﾚdocProps/core.xml｢(�QOﾂ0ﾇﾟMKﾟG;.c$jx墜ﾄ腔ｵ=ｲvM[¦{ｻ

&ｾ ﾝｿﾍY{0VTj�A(Vq｡ﾖ3 ,ﾂ)

ｬ｣鑑ｲR0CG-h槧ﾞdLｧｬ2 *

ﾆ -')2=C輻干e赤湿B ｪ2:5ﾖ芭 粐(ｧ寂龠�Hﾎz､ﾞ甸p� ﾊY"¦ﾑ:0ﾒﾙﾐVｮ燃ｸ｣;敞ｽfsﾖ{ 蛙Xﾗ 杓

1�X>ｿｶｫ�5^1@yﾆY黻+!ﾏ 鎔v

ﾌu>fｺﾊ腆ﾛp濤pｬ+ﾃｭDｾ宴eFh艝ｯ#^]R�9W ｱN6wﾘ区 i%}i}�x'ﾒﾎｷs=~¦*(塗$ﾇｹK紵ﾉﾈgｳﾌｿqｦKﾈﾓXｧa$I脯!閟

ﾆPK!S4ﾂ隔word/fontTable.xmlﾌ瞥nﾚ@�放ﾖ章^@T､｢ｪMｭ x${ﾆ8l/ｾ.ﾒｾA髭+ｵｪ/ｳﾞｭ_｡ﾇ茁Rｺ#9> ?gﾎ/n=W

嶢@2ﾁ嵎8ﾃH｣ﾜﾆGM ｺ B啜+8m｢)戊｢ ﾅyﾘ

ｮ､�lM(7t]ﾚ <>06；

Fｺ儁_{�ｮt罨P(xｶt/Q-<&Z(ａ妍 ﾉznﾏ#献V慢68 �0#ﾞ鱈�ﾂ�君維Dｸ､ﾇ1l潮 3芙ﾄc羨･蝶ｩ3e;+yBFn\l6ａ

ｱｼﾁ �ｩb ﾅ<牢ﾚU$七ｵ

圧ﾙ�:@ﾍｿE ﾚ肅O譲_ﾄUW@i富ｽﾖgﾜvV巓テbWq例ｷ-\ﾂ藹Xﾎ条ZCvK�ﾚ ﾌNoMjukｽnｯ)kT7恚*獅q=鋭<ｪk

覯ｩ]ﾑP{陸ｳﾜ 乾(ﾊ5q燗pｶ∀ｶUﾛﾙｶlMC>lc｣w".ﾔ8俶V ｪ �ｳ粋ｭ∀mｷ}oｬ"oﾀ售ｽ ｴ-贄!Z�P幅�r y l

ﾉ|lQﾆﾆ P､ｵXﾝﾇrLﾉ､ｫ/動ｻ,g?無淪ｻｻ褌｡ﾇ\

0;k=&��ﾓﾖﾐﾋ&ﾓ�ﾂ}ﾂ:q歎})ﾀ;JNｫﾝcl�ﾊ�醴3ｷ野眺ｿPK!-a docProps/app.xml｢(彜ﾁn1ｽ#ｵｽ7NB(i4q�｡

Fﾊｶ=�b盞-ﾛ種眸G1ﾆﾙ&q{z v�-\>ｶｺX｣ﾊ喨9頷ﾋ唆ｵ2ﾋiy[}8勇按ﾔB[φr｢ｼ莕_ﾁﾜ[>*ｭ0aZｮbtﾆ�a+B詳:

索ｭ�%ｳM｣$^Y ｢瑛ﾘ�3¦敬jｬﾏﾜaaﾙm悽.ｭｭL惲]ｵq$呂�ﾓ""應鐃mc�Be｣ﾐ彬ﾇﾔ80K--ﾀｽ 瑠sb:ｩ呆BF .ﾞ

eｼwN+)"ﾙﾋ?)鶩-M,nvFi-¦ﾈﾊｯ竊 %¦T�瑚6/某ｸUbｳRh恆ｼ: -#ﾗ(ﾒﾎ"ﾉ-雌5ﾊh}ﾔ7ｺ賖Y¦都ﾓr-ｼ&茶iｬ+vXｻ=ﾟ

>ﾚ>ﾘ>ﾟ>F#ｽ�t遮�V%p:佇N

5NEV*j7

}b�襤ｮyｧ｡S慄/珮?ｶﾎl�ﾙ ｮ&ﾏｿ�Wﾙｫ麦/O/,*ｮNﾈ曝wc簡1

Yｬ駭\難^ｧS饐ｳﾄz? #�ｮ諡 ﾘ�ｳKﾓ椒D)PK-! "ｭ[Content_Types].xmlPK-!ｷNﾆ_rels/.relsPK-!6H鰭

ｾword/_rels/document.xml.relsPK-!ﾓ!ﾌｯL word/document.xmlPK-!�sUtﾟN+word/footnotes.xmlPK-

!@!¦uﾙ,word/endnotes.xmlPK-!{oR.word/theme/theme1.xmlPK-!e-6ceyc5word/settings.xmlPK-!ｿﾘ樺

ｻ:word/webSettings.xmlPK-!｡ﾃﾈxD;word/styles.xmlPK-!鑁Tﾒﾘｪ

&Eword/numbering.xmlPK-!N$鋇xﾚ.HdocProps/core.xmlPK-!S4ﾂ隔ﾝJword/fontTable.xmlPK-!-a

�docProps/app.xmlPKｵP