	TRACK 1	TRACK 2	TRACK 3
	DAY 1 (Sunday, Nov. 20)		
8:00AM-9:00AM	**REGISTRATION**		
9:00-10:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
10:30-11:00	**Tea Break**		
11:00-12:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
12:30-2:00	**Lunch Break**		
2:00-3:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
3:30-4:00	**Tea Break**		
4:00-5:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
	DAY 2 (Monday, Nov. 21)		
7:30AM-9:00AM	**REGISTRATION**		
9:00-11:00	**Plenary Session** **Inauguration** **General Chair's Address** **Program Chair's Address** **Plenary Keynote 1: Giovanni Demicheli, EPFL - "Nanosystems: devices, circuits, architectures and applications"** **Plenary Keynote 2: Janusz Rajski, Mentor Graphics - "The Future of Test – an EDA/DFT Perspective"**		
11:00 - 11:30	**Tea/Coffee Break**		
11:30 - 13:00	**Session A1: Testing Clock and Timing** ***Moderator: Pramod Notiyath, Synopsys*** 1. On Detecting Transition Faults in the Presence of Clock Delay Faults Yoshinobu Higami, Hiroshi Takahashi, Shin-Ya Kobayashi and Kewal Saluja 2. Testing of Clock-Domain Crossing Faults in Multi-Core System-on-Chip Naghmeh Karimi, Zhiqiu Kong, Krishnendu Chakrabarty, Pallav Gupta and Srinivas Patil 3. On-Chip Programmable Dual-Capture for Double Data Rate Interface Timing Test and Validation Hyunjin Kim and Jacob Abraham 4. Time Domain Characterization and Test of High Speed Signals Using Incoherrent Subsampling, Debesh Bhatta, Josh W Wells and Abhijit Chatterjee	**Session B1: Post-Silicon Debug and Validation** ***Moderator: Said Hamdioui, Delft Univ.*** 1. Post-Silicon Timing Validation Method using Path Delay Measurements Eun Jung Jang, Jaeyong Chung, Anne Gattiker, Sani Nassif and Jacob Abraham 2. Backward Reasoning with Formal Properties: A methodology for bug isolation on simulation traces Anvesh Komuravelli, Srobona Mitra, Ansuman Banerjee and Pallab Dasgupta 3. Design of a Test Processor for Asynchronous Chip Test Steffen Zeidler, Christoph Wolf, Milos Krstic, Frank Vater and Kraemer Rolf 4. On generating vectors for accurate post-silicon delay characterization Prasanjeet Das and Sandeep Gupta	**Special Session C1: Memory BIST Advances for Nanoscale Technologies** ***Organizer/Moderator: V. R. Devanathan, Texas Instruments*** **1. Physical-aware Memory BIST Datapath Synthesis: Architecture and Case -studies on Complex SoCs** **V. R. Devanathan, Sunil Bhavsar, Rajat Mehrotra (Texas Instruments)** **2. Failure Analysis and Test Solutions for Low-Power SRAMs** **L. B. Zordan, A. Bosio,, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel (LIRMM), N. Badereddine (Intel)** **3. A Robust Solution for Embedded Memory Test and Repair** **K. Darbinyan, G. Harutyunyan, S. Shoukourian, V. Vardanian, Y. Zorian (Synopsys)**
13:00 -14:00	**Lunch Break**		
14:00 -15:30	**Session A2: Power Aware Testing I** ***Moderator: Artur Pogiel, Mentor Graphics*** 1. Temperature Dependent Test Scheduling for Multi-core System-on-Chip Chunhua Yao, Kewal Saluja and Parameswaran Ramanathan 2. Test Scheduling for Multicore SoCs with Dynamic Voltage Scaling and Multiple Voltage Islands, Chrysovalantis Kavousianos, Krishnendu Chakrabarty, Arvind Jain and Rubin Parekhji 3. Selective Test Response Collection for Low-Power Scan Testing	**Session B2: Test Compression Techniques** ***Moderator: Tomoo Inoue, Hiroshima City U.*** 1. Predicting Scan Compression IP Configurations to Match the IP to the Design for Better QoR Rohit Kapur 2. Low Test Data Volume Low Power At-Speed Delay Tests Using Clock-Gating Elham Moghaddam, Janusz Rajski and Sudhakar Reddy 3. Test Compression Based on Lossy Image Encoding Hideyuki Ichihara, Yuka Iwamoto, Yuki Yoshikawa and Tomoo Inoue	**Special Session C2: Advanced Test Topics I** ***Moderator: Rajesh Gupta, Univ. of California (San Diego)*** **1: Memory technologies and test their test challenges Speaker: Manuel D'Abreu, Sandisk** **2: High Level Verification and its Use at Post-Silicon Debugging and Patching Speaker: Masahiro Fujita, Univ. of Tokyo**

	Dong Xiang 4. Low Power Test-Compression for High Test-Quality and Low Test-Data Volume Vasileios Tenentes and Chrysovalantis Kavousianos	4. Multiscan-based Test Data Compression Using UBI Dictionary and Bitmask Yang Yu, Gang Xiang and Liyan Qiao	
15:30 - 16:00	**Tea/Coffee Break**		
16:00 - 17:30	**Session A3: Advanced Design for Testability Techniques** ***Moderator: Nagesh Tamarapalli, AMD*** 1. Multi-Cycle Test with Partial Observation on Scan-Based BIST Structure Yasuo Sato, Seiji Kajihara, Hiaso Yamaguchi and Makoto Matsuzono 2. SSTKR: Secure and Testable Scan Design Through Test Key Randomization Mohammed Abdul Razzaq, Virendra Singh and Adit Singh 3. An Innovative Methodology for Scan Chain Insertion and Analysis at RTL Lilia Zaourar, Yann Kieffer and Chouki Aktouf 4. Adaptation of Standard RT Level BIST Architectures to System Level Designs Nastaran Nemati and Zainalabedin Navabi	**Session B3: Advanced Techniques in Fault Diagnosis I** ***Moderator: Sandeep Gupta, Univ. of Southern California*** 1. Diagnostic Test of Robust Circuits Alejandro Cook, Sybille Hellebrand, Thomas Indlekofer and Hans-Joachim Wunderlich 2. An Accurate Timing-aware Diagnosis Algorithm for Multiple Small Delay Defects Po-Juei Chen, Wei-Li Hsu, James C.-M. Li, Nan-Hsin Tseng, Kuo-Yin Chen, Wei-Pin Changchien and Charles C. C. Liu 3. Diagnosis of Multiple Scan-Chain Faults in the Presence of System Logic Defects, Zhen Chen, Sharad Seth, Dong Xiang and Bhargab Bhattacharya 4. Diagnosing Multiple Slow Gates for Performance Tuning in the face of Extreme Process Variations, Xi Qian, Adit Singh and Abhijit Chatterjee	**Special Session C3: 3D Integrated Circuits: Design, Test, and Yield** ***Organizer/Moderator: Krishnendu Chakrabarty, Duke Univ.*** **1. Design of 3D-Specific Systems: Medium- and Long-Term Perspectives** **Paul Franzon (North Carolina State University)** **Speaker: Paul Franzon** **2. Testing and Design-for-Testability Techniques for 3D Integrated Circuits** **Brandon Noia and Krishnendu Chakrabarty (Duke University)** **Speaker: Krishnendu Chakrabarty** **3. Yield Improvement and Test Cost Optimization for 3D Stacked ICs** **Said Hamdioui (Delft University of Technology)** **Speaker: Said Hamdioui**
END OF DAY 2			
DAY 3 (Tuesday, Nov. 22)			
7:30AM-8:30AM	**REGISTRATION**		
8:30 - 9:15	**Distinguished Lecture 1:** **Rubin Parekhji, Texas Instruments - "Managing Test Cost and Test Quality on Large SOCs – Different Product Perspectives"** ***Moderator: Susmita Sur-Kolay, ISI***		
9:30 - 11:00	**Session A4: Power Aware Testing II** ***Moderator: Nilanjan Mukherjee, Mentor Graphics*** 1. Rewind-Support for Peak Capture Power Reduction in Launch-Off-Shift Testing Ozgur Sinanoglu 2. Low Power Decompressor and PRPG with Constant Value Broadcast Jerzy Tyszer, Michal Filipek, Yoshiaki Fukui, Hiroyuki Iwata, Grzegorz Mrugalski, Janusz Rajski and Masahiro Takakura 3. Effective Launch-to-Capture Power Reduction for LOS Scheme with Adjacent-Probability-Based X-Filling Kohei Miyase, Yuta Uchinodan, Kazunari Enokimoto, Yuta Yamato, Xiaoqing Wen, Seiji Kajihara, Fangmei Wu, Luigi Dilillo, Alberto Bosio, Patrick Girard and Arnaud Virazel 4. Virtual Circuit Model for Low Power Scan Testing in Linear Decompressor-based Compression Environment Zhen Chen, Jia Li, Dong Xiang and Yu Huang	**Session B4: Test Quality Improvement Techniques** ***Moderator: Xiaowei Li, Institute of Computing Technology - CAS*** 1. A Process Monitor Based Speed Binning and Die Matching Algorithm Sreejit Chakravarty 2. Optimized Test Error Detection by Probabilistic Retest Recommendation Models Matthias Kirmse and Uwe Petersohn 3. Adaptive Test Framework for Achieving Target Test Quality at Minimal Cost Baris Arslan and Alex Orailoglu 4. A Fault Criticality Evaluation Framework of Digital Systems for Error Tolerant Video Applications, Yuntan Fang, Huawei Li and Xiaowei Li	**Special Session C4: Advanced Test Topics II** ***Moderator: Nicco (Shaleen) Bhabu, Cadence*** **1. Integrated Design & Test: Conquering the Conflicting Requirements of Low-Power, Variation-Tolerance, and Test Cost** **Ashish Goel, Swaroop Ghosh, Mesut Meterelliyoz (Purdue U) Jeff Parkhurst (Intel) and Kaushik Roy (Purdue U) Speaker: Kaushik Roy**
11:00 - 11:30	**Tea/Coffee Break**		
11:30 - 13:00	**Session A5: Defect Based Test Techniques** ***Moderator: Xiaoqing Wen, Kyushu Institute of Tech.*** 1. Test Pattern Selection for Defect-Aware Test Yoshinobu Higami, Hiroshi Furutani, Takao Sakai, Shuichi Kameyama and Hiroshi Takahashi 2. Efficient SAT-Based Search for Longest Sensitisable Paths Matthias Sauer, Jie Jiang, Alexander Czutro, Ilia Polian and Bernd Becker 3. Mapping Transaction Level Faults to Stuck-at Faults in Communication Hardware Fatemeh Javaheri, Majid Namaki-Shoushtari, Parastoo Kamranfar and Zainalabedin Navabi 4. On Generation of 1-Detect TDF Pattern Set with Significantly Increased SDD Coverage Fang Bao, Ke Peng, Krishnendu Chakrabarty and Mohammad Tehranipoor	**Session B5: Advanced Memory Test Techniques I** ***Moderator: Yasuo Sato, Kyushu Institute of Tech.*** 1. Efficient Use of Unused Spare Columns to Improve Memory Error Correcting Rate Umair Ishaq, Jihun Jung, Jaehoon Song and Sungju Park 2. New Fault Detection Algorithm for Multi-Level Cell Flash Memories Jaewon Cha, Ilwoong Kim and Sungho Kang 3. A New Test Paradigm for Semiconductor Memories in the Nano-Era Said Hamdioui, Venkataraman Krishnaswami, Ijeoma Sandra Irobi and Zaid Alars 4. On Defect Oriented Testing for Hybrid CMOS/memristor Memory Nor Zaidi Haron and Said Hamdioui	**Special Session C5: Robust Systems Research Around the Globe** ***Chair: Prof. Subhasish Mitra, Stanford University*** **1. Dependable VLSI Program in Japan: Program overview and the curent status of dependable VLSI platform project** **Prof. Hidetoshi Onodera (Kyoto U)** **2. Reliability: A Cross-Disciplinary and Cross-Layer Approach** **Prof. Norbert Wehn (University of Kaiserslautern)** **3. Underdesigned and Opportunistic Computing** **Prof. Puneet Gupta (UCLA) and Prof. Rajesh Gupta (UCSD)**
13:00 -14:00	**Lunch Break**		

14:00 - 18:00PM	SOCIAL PROGRAM		
18:450-19:30PM	Banquet Keynote: Sandeep Sinha (Lumis Partners)		
19:30PM-20:00	BANQUET AWARDS AND ANNOUNCEMENTS		
20:00PM+	BANQUET DINNER		
DAY 4 (Wednesday, Nov. 23)			
7:30AM-8:30AM	REGISTRATION		
8:30 - 9:15	Distinguished Lecture 2: **Gordon Roberts, McGill University - "Time-Mode Signal Processing and Its Impact On Analog/Mixed-Signal/RF Testing"** *Moderator: Adit Singh, Auburn U.*		
9:30 - 11:00	**Session A6: Advanced Techniques in Online Testing** ***Moderator: Kazumi Hatayama, Nara Institute of Science and Technology*** 1. Yield-per-area optimization for 6T-SRAMs using an integrated approach to exploit spares and ECC to efficiently combat high defect and soft-error rates Jae Chul Cha and Sandeep Gupta 2. A Hybrid Fault Tolerant Architecture for Robustness Improvement of Digital Circuits Duc Anh Tran, Arnaud Virazel, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch and Hans-Joachim Wunderlich 3. A new Architecture to Cross-Fertilize On-line and Manufacturing testing, Paolo Bernardi and Matteo Sonza Reorda 4. Online Test Macro Scheduling And Assignment In MPSoC Design Behnam Khodabandehloo, Seyed Alireza Hoseini, Sajjad Taheri, Mohammad Hashem Haghbayan, Mahmood Reza Babaei and Zeinolabedin Navabi	**Session B6: Advanced Techniques in RF/Mixed Signal Testing** ***Moderator: Michiko Inoue, Nara Institute of Science and Technology*** 1. Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs Manuel J. Barragan, Rafaella Fiorelli, Gildas Leger, Adoracion Rueda and Jose Luis Huertas 2. On Replacing an RF Test with an Alternative Measurement: Theory and a Case Study, Alexios Spyronasios, Louay Abdallah, Haralampos-G. Stratigopoulos and Salvador Mir 3. Test and Diagnosis of Analog Circuits using Moment Generating Functions Suraj Sindia, Vishwani Agrawal and Virendra Singh 4. Mixed-signal fault equivalence: search and evaluation Nuno Guerreiro and Marcelino Santos	**Special Session C6: Power-Aware Testing and Test of Low Power Designs** ***Organizer/Moderator: Patrick Girard, LIRMM*** **1. Power Aware Shift and Capture ATPG methodology for Low Power Designs** **S. Khullar, S. Bahl (STMicroelectronics)** **Speaker: S. Khullar** **2. Power-Aware Test Pattern Generation for At-Speed LOS Testing** **A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM), K. Miyase, X. Wen (Kyushu Institute of Technology)** **Speaker: A. Bosio** **3. Power Aware Embedded Test** **X. Lin, E. Moghaddam, N. Mukherjee B. Nadeau-Dostie, J. Rajski (Mentor Graphics), J. Tyszer (Poznan University of Technology)** **Speaker: N. Mukherjee**
11:00 - 11:30	Tea/Coffee Break		
11:30 -13:00	**Session A7: Innovative Techniques in Microprocessor Testing** ***Moderator: Srikanth Venkataraman, Intel.*** 1. Distributed Comparison Test Driven Multiprocessor Speed-Tuning: Targeting Performance Gains Under Extreme Process Variations Jayaram Natarajan, Abhijit Chatterjee and Adit Singh 2. An Online Mechanism to Verify Datapath Execution using Existing Resources in Chip Multiprocessors, Rance Rodrigues and Sandip Kundu 3. An Efficient 2-Phase Strategy to Achieve High Branch Coverage Sarvesh Prabhu, Michael Hsiao, Saparya Krishnamoorthy, Loganathan Lingappan, Vijay Gangaram and Jim Grundy 4. Soft error recovery technique for multiprocessor SOPC Uroš Legat, Anton Biasizzo and Franc Novak	**Session B7: Test Automation and Analysis** ***Moderator: Subhasish Mukherjee (Cadence)*** 1. Efficient BDD-based Fault Simulation in Presence of Unknown Values Michael Kochte, Sandip Kundu, Kohei Miyase, Xiaoqing Wen and H.-J. Wunderlich 2. Analysis of Resistive Bridge Defect Delay Behavior in the Presence of Process Variation Shida Zhong, Saqib Khursheed, Bashir Al-Hashimi, Sudhakar Reddy and Krishnendu Chakrabarty 3. Automation of 3D DfT Insertion, Sergej Deutsch, Vivek Chickermane, Brion Keller, Subhasish Mukherjee, Mario Konijnenburg, Erik Jan Marinissen and Sandeep K. Goel 4. MarciaTesta: an EDA tool for the automatic generator of test program for microprocessor data caches, Marco Indaco	**Special Session C7: Post-Si Debug and Validation** ***Moderator: Rubin Parekhji, Texas Instruments*** **Invited Talk 1. Sneak peek at growing HVM Test and Debug challenges associated with Ring Architecture based Intel® Xeon® Processor** **Speaker: Shridhar Bendi, Intel** **Invited Talk 2. Structured Silicon Debug: Key for** **Reducing Time to Production Speaker: Srinivas Vooka, Texas Instruments**
13:00 -14:00	Lunch Break		
14:00 - 15:30	**Session A8: 3D IC Testing** ***Moderator: Indranil Sengupta, IIT - Kharagpur*** 1. Wrapper Chain Design for Testing TSVs Minimization in Circuit-Partitioned 3D SoC Yuanqing Cheng, Lei Zhang, Yinhe Han, Jun Liu and Xiaowei Li 2. Identification of Defective TSVs in Pre-Bond Testing of 3D ICs Brandon Noia and Krishnendu Chakrabarty 3. A Unified Interconnects Testing Scheme for 3D Integrated Circuits Chih-Yun Pai, Liang-Bi Chen, Bo-Chuan Cheng, Jie-Chi Chen, Katherine Shu-Min Li and Ji-Jan Chen 4. Cost-Effective TSV Grouping for Yield Improvement of 3D-ICs Yi Zhao, Saqib Khursheed and Bashir Al-Hashimi	**Session B8: Advanced Memory Test Techniques II** ***Moderator: Seiji Kajihara, Kyushu Institute of Technology*** 1. Test for Parasitic Memory Effect in SRAMs Ijeoma Sandra Irobi, Zaid Alars, Said Hamdioui and Claude Thibeault 2. Transient Noise Failures in SRAM Cells: Dynamic Noise Margin Metric Elena Ioana Vatajelu, Álvaro Gómez-Pau, Michel Renovell and Joan Figueras 3. Fault Diagnosis in Memory BIST Environment with Non-March Tests Jerzy Tyszer, Grzegorz Mrugalski, Artur Pogiel, Nilanjan Mukherjee, Janusz Rajski and Pawel Urbanek 4. Characterizing Pattern Dependent Delay Effects in DDR Memory Interfaces, Atul Gupta, Ajay Kumar and Manas Chhabra	**Special Session C8: Embedded Tutorial - Testability of Cryptographic Hardware and Detection of Hardware Trojans** ***Moderator: Jacob Abraham, University of Texas, Austin*** **Speakers: Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, IIT Kharagpur**

		Manas Chhabra	
15:30 - 16:00	**Tea/Coffee Break**		
16:00 - 17:30	**Session A9: Advanced Techniques in Fault Diagnosis II** ***Moderator: Huawei Li, Institute of Computing Technology*** 1. Improved Fault Diagnosis for Reversible Circuits Hongyan Zhang, Robert Wille and Rolf Drechsler 2. Embedded Test for Highly Accurate Defect Localization, Abdullah Mumtaz, Michael E. Imhof, Stefan Holst and Hans-Joachim Wunderlich 3. On Using Design Partitioning To Reduce Diagnosis Memory Footprint Xiaoxin Fan, Huaxing Tang, Sudhakar M. Reddy, Wu-Tung Cheng and Brady Benware 4. Exploring Impact of Faults on Branch Predictors' Power for Diagnosis of Faulty Module, Gunjan Bhattacharya, Ilora Maity, Baisakhi Das and Biplab K Sikdar	**Session B9: Innovative DFT Solutions** ***Moderator: Kenneth Pichamuthu, IBM*** 1. Breaking the Test Application Time Barriers in Compression: Adaptive Scan – Cyclical (AS-C) Anshuman Chandra, Jyotirmoy Saikia and Rohit Kapur 2. Exploiting Free LUT Entries to Mitigate Soft Errors in SRAM-based FPGAs Keheng Huang, Yu Hu and Xiaowei Li 3. A Single-Configuration Method for Application-Dependent Testing of SRAM-based FPGA Interconnects Thulasiraman Nandhakumar, Haider Almurib and Fabrizio Lombardi 4. Multi-Visit TAMs to Reduce the Post-Bond Test Length of 2.5D-SICs with a Passive Silicon Interposer Base Chun-Chuan Chi, Erik Jan Marinissen, Sandeep Kumar Goel and Cheng-Wen Wu	**Session C9: Board and System Level Testing** ***Moderator: Erik Larsson, Linkoping University*** 1. Test Scheduling in an IEEE P1687 Environment with Resource and Power Constraints Farrokh Ghani Zadegan, Urban Ingelsson, Golnaz Asani, Gunnar Carlsson and Erik Larsson 2. Automatic SoC Level Test Path Synthesis Based on Partial Functional Models Anton Tsertov, Artur Jutman, Sergei Devadze and Raimund Ubar 3. A Boundary Scan Circuit with Time-to-Digital Converter for Delay Testing Hiroyuki Yotsuyanagi, Hiroyuki Makimoto and Masaki Hashizume 4. Burst-Mode Transmission and Data Recovery for Multi-GHz Optical Packet Switching Network Testing Carl Gray, David Keezer, Howard Wang and Keren Bergman