LATEST NEWS NEW!

Conference Registration is now open.
ATS 20th Anniversary Compendium of Papers
Final Submissions now accepted: Author Kit
IMPORTANT: Hotel Reservation & Visa Application Information.

About this conference

20th ATS 2011 is the twentieth in this series of symposia started in 1992 devoted to testing, fault tolerant computing and the design of reliable circuits and systems. ATS is recognized as the main event in Asia that covers the many dimensions of testing and fault-tolerance. In 2011, the 20th Anniversary of the Asian Test Symposium will be celebrated in New Delhi, India and is of particular sinificance due to the rise of Asia, over the last several decades, in the areas of integrated circuit design and manufacturing, and electronic systems and software engineering, both of which embrace testing as a core technology. New Delhi, in particular, is a major player in India's computing industry with emerging "technology satellites" in nearby Noida and Gurgaon and the face of her new "modernity". At the same time, New Delhi, is the centerpiece of Indian culture, tradition and cuisine, having been at the helm of Indian history for centuries, dating back to the Mughal period and the British Raj.

Symposium Theme

The theme for ATS 2011 will be **"Test Odyssey 2020: Testing Systems and Devices at the Peta and Nano Scales"**. This theme is inspired by the fact that technology is trending towards extremely high levels of integration at the package and chip levels, very high speeds of operation (> 100 GHz) and use of deeply scaled technology (approaching 10nm CMOS). In addition, a key test challenge will arise due to the ability to design complex systems such as robots that encompass sensors, communications systems, processors, transducers and enabling software. In addition to passing post-manufacture test procedures, such systems and relevant devices must exhibit fault-tolerance and survivability characteristics.

Topics of Interest (but are not limited to)

Original contributions in testing, fault tolerant and reliable computing are solicited. Topics of interest include, but are not limited to, the following categories:

Automatic Test Pattern Generation (ATPG)	Boundary Scan
Test Compression	Online Test
Temperature/Power-aware Test	Design-for-testability (DFT)
Microprocessor Test	Mixed signal and Analog Test
Memory Test	System-in-package (SiP)/ 3D Test
Test Quality and Reliability	Design Validation/Silicon Debug
Fault Modeling/Defect Based Test	Fault Simulation/Diagnosis
Software Testing	Board and System Test
Other	

Important Dates/Deadlines

Papers	~~May 27~~ June 10, 2011
Special Session proposals	~~June 3~~ June 17, 2011
Tutorial proposals	~~June 3~~ June 17, 2011
Exhibition/Booth proposals	~~May 27~~ June 10, 2011
Notification of acceptance	~~August 1~~ August 15, 2011
Camera-ready paper due date	~~August 22 September 5~~ September 20, 2011

Technical Co-Sponsors

Gold Sponsors

Silver Sponsors

Conference Registration Fee Structure

One author of each paper must be registered for the conference.

If an author is presenting 2 or 3 papers in which he/she is a co-author, that author MUST register at the full conference rate and not the student rate.

FOR DELEGATES RESIDENT OUTSIDE INDIA, FEE IN US $
FOR DELEGATES RESIDENT IN INDIA, FEE IN INDIAN RUPEES

Registration Fees (US $, Indian Rupees)	Symposium		Tutorial 1 or Tutorial 2		WRTLT		Subtotal
	Until November 11, 2011	After November 11, 2011	Until November 11, 2011	After November 11, 2011	Until November 11, 2011	After November 11,2011	
DELEGATE	$575 Rs. 27025	$675 Rs. 31725	$100 Rs. 4700	$145 Rs. 6815	$275 Rs. 12925	$325 Rs. 15275	
STUDENT DELEGATE	$275 Rs. 12925	$325 Rs. 15275	$50 Rs. 2350	$70 Rs. 3290	$140 Rs. 6580	$165 Rs. 7755	
Extra Social Programme Tickets*	[$ 70] .....each X .....ticket(s) [Rs. 3290] .....each X .....ticket(s)						
Extra Page Charges for authors	[$ 100] .....per page X .....page(s) [Rs. 4700] .....per page X .....page(s)						
Total							

*Registration fee for DELEGATES includes social event tickets. STUDENT fee **does not include** the social event (the reception, the tour and the banquet).

VSI Fellowship

Please apply for the VSI Fellowship using the following application form: VSI Fellowship form

Deadline for fellowship application is **November 11, 2011**

Please email the completed forms to the ATS Finance Team:

Virendra Singh {virendra@computer.org} ,

Shyam Nagpal {shyamnagpal@icesindia.com, shyamnagpal@gmail.com}

Amit Patra {amit@ee.iitkgp.ernet.in}

Registration Payment

Registration to the ATS 2011 conference can be done in two ways:

A. Online Registration using Credit Cards / Debit Card/Net Banking/Itz Cash Cards. Please click on the link below:

REGISTER & PAY NOW NEW!

B. Fill-in the registration form and send your form and payment by bank draft in favour of **'*Asian Test Symposium 2011*'** to Shyam Nagpal (address, fax & email below)

Technical Co-Sponsors

Gold Sponsors

Silver Sponsors

Shyam Nagpal
Event Manager, ATS 2011 &
Managing Director, International Conference and Exhibition Services (ICES) Pvt. Ltd.
23, Bhawani Kunj, Sector D-2,
Vasant Kunj, New Delhi -110070, India
Phone: + 91-11-2613-3870, Fax: +91-11-2613-4172
Email : shyamnagpal@icesindia.com, shyamnagpal@gmail.com
Website: www.icesindia.com

ATS 2011 Organizing Committee| ats2011_orgcomittee@yahoogroups.com

The **ATS 20th anniversary compendium of selected papers** celebrates the 20th anniversary of the Asian Test Symposium. This collection of papers have been chosen by the selection committee to represent the best contributions among those presented in ATS in past 10 years, based on their impact in the field of testing.

The **ATS compendiums of selected papers** remind the audiences of the tremendous progress that has been made in the field of testing in the past twenty years. This progress mirrors the rise of semiconductor research in Asia.

The **ATS 20th anniversary compendium of selected papers** charts the 2nd decade of progress in test research and is an invaluable guide for researchers, students and practitioners alike.

Previously, the **ATS 10th anniversary compendium of selected papers** was published in 2001 to mark the first decade of progress in test research.

Links

- ATS 20th anniversary compendium of selected papers
- ATS 10th anniversary compendium of selected papers
- ATS 20th anniversary compendium selection committee
- ATS 10th anniversary compendium selection committee

Technical Co-Sponsors

Gold Sponsors

Silver Sponsors

ATS 2011 Organizing Committee| ats2011_orgcomittee@yahoogroups.com

Important Dates/Deadlines

Papers	~~May 27~~ June 10, 2011
Special Session proposals	~~June 3~~ June 17, 2011
Tutorial proposals	~~June 3~~ June 17, 2011
Exhibition/Booth proposals	~~May 27~~ June 10, 2011
Notification of acceptance	~~August 1~~ August 15, 2011
Camera-ready paper due date	~~August 22~~ ~~September 5~~ September 20, 2011

Author Guidelines

Paper Presentation Template

NEW!

Please use the following template for presentation of your paper.

Paper Submission Instruction

The following is a URL link to the "Author's Final Paper Formatting and Submission Instructions" Webpage (Online Author Kit) for 2011 Asian Test Symposium (ATS 2011): Author Kit

Please note: The Author Kit's PDF eXpress service will not be available immediately. The PDF eXpress service will be available on or after Tuesday, **30 August 2011** and that the paper submission deadline has been extended to **Tuesday, 20 September 2011**.

Paper Formatting Instructions

Please format your paper using the IEEE Conference style in US letter size. Templates are provided below. Make sure that page numbers are removed. The nominal page limit is 6. Up to 4 additional pages can be purchased at **$100/page**. The excess page charges need to be paid during the registration process.

Microsoft Word Template
If you are using Microsoft Word, please use this template.

Latex Templates
If you are using latex, you can use the templates from here.

NOTE: Blind review is optional.

Electronic Submission

The paper submission process uses EasyChair conference manager. Papers should be submitted in ***PDF format***. Please click on the EasyChair link to access the submission system.

Paper acknowledgments will be sent to all authors.

IEEE Copyright Form
All authors must complete copyright transfer in order to have their papers included in the ATS program. All clearances for publication must be obtained by the authors. Instructions for copyright transfer will be sent to authors of accepted papers.

Paper Topics

Choose from one of the following categories:

Automatic Test Pattern Generation (ATPG)	Boundary Scan
Test Compression	Online Test
Temperature/Power-aware Test	Design-for-testability (DFT)
Microprocessor Test	Mixed signal and Analog Test
Memory Test	System-in-package (SiP)/ 3D Test

Technical Co-Sponsors

Gold Sponsors

Silver Sponsors

Test Quality and Reliability	Design Validation/Silicon Debug
Fault Modeling/Defect Based Test	Fault Simulation/Diagnosis
Software Testing	Board and System Test
Innovative Industrial Test Practices*	Other

* In above list of categories, ATS 2011 has introduced a new category for technical papers to solicit original contributions that showcase *Innovative Industrial Test Practices*. Submissions could be related to silicon test data studies, new/novel test EDA tool user experiences, or case studies. Submission requirements and review guidelines for these papers are the same as regular technical papers.

Special Sessions

Please see separate deadlines. All special session submissions are also handled using the EasyChair system. Please choose from one of the following categories. For, industrial test practices paper guidelines is as above. Proposals related to panels/special sessions, embedded tutorials, and full/half day tutorials are limited to 3 pages, and should detail abstract and bulleted list of topics, targeted audience, proposed duration, organizer's name and affiliation, speakers' names, affiliations, short bios, and approval status for participation at ATS 2011.

Special Session Proposal

Embedded Tutorial Proposal

Full/Half Day Tutorial Proposal

ATS 2011 Organizing Committee| ats2011_orgcomittee@yahoogroups.com

HOTEL INFORMATION

The Venue for 20th Asian Test Symposium is Hotel Crowne Plaza, Okhla, New Delhi.

The Organising Committee has done block booking of the rooms at special rates for convenience of the delegates.

Rooms in Hotel Crowne Plaza are no longer available, Alternate arrangement for rooms have been made at Hotel Eros (manager by Hilton), Nehru Place, New Delhi. This hotel is 15minutes from the conference venue.

Room rates

Single Room: Rs. 8000 + Taxes

Double Room: Rs. 9000 + Taxes

The above rate includes aiport transfers and buffet breakfast.

Please contact Hotel Eros, for any assistance you may need for your hotel reservation.

Vibhu Wadhwa
Reservations Executive
EROS Hotel managed by Hilton
Nehru Place, New Delhi – 110019, India
Tel +91 11 4133 1710 Fax +91 11 2622 2810 |
Vibhu.wadhwa@hilton.com |
www.hilton.com

Please contact Mr. Shyam Nagpal [shyamnagpal@icesindia.com] for any queries pertaining to reservations.

IMPORTANT VISA INFORMATION

All foreign visitors need to obtain an Indian Visa for travel to India. For visa related details, please contact the nearest Indian Embassy or Consulate in your Country. Should you require an invitation letter for visa, the Organizing Committee of ATS-2011, will be happy to send one.

Please send your passport details to **Mr. Shyam Nagpal** [shyamnagpal@icesindia.com] for issuance of invitation letter.

Since the visa process for India is lengthy, you are requested to initiate the visa process urgently.

Name ……(As on Passport)

Nationality ……..

Passport Number……

Place of Issue……..

Date of Issue……..

Passport valid till ……..

Technical Co-Sponsors

Gold Sponsors

Silver Sponsors

NEW!

LATEST NEWS

Conference Registration is now open.
ATS 20th Anniversary Compendium of Papers
Final Submissions now accepted: Author Kit
IMPORTANT: Hotel Reservation & Visa Application Information.

About this conference

20th ATS 2011 is the twentieth in this series of symposia started in 1992 devoted to testing, fault tolerant computing and the design of reliable circuits and systems. ATS is recognized as the main event in Asia that covers the many dimensions of testing and fault-tolerance. In 2011, the 20th Anniversary of the Asian Test Symposium will be celebrated in New Delhi, India and is of particular sinificance due to the rise of Asia, over the last several decades, in the areas of integrated circuit design and manufacturing, and electronic systems and software engineering, both of which embrace testing as a core technology. New Delhi, in particular, is a major player in India's computing industry with emerging "technology satellites" in nearby Noida and Gurgaon and the face of her new "modernity". At the same time, New Delhi, is the centerpiece of Indian culture, tradition and cuisine, having been at the helm of Indian history for centuries, dating back to the Mughal period and the British Raj.

Symposium Theme

The theme for ATS 2011 will be **"Test Odyssey 2020: Testing Systems and Devices at the Peta and Nano Scales"**. This theme is inspired by the fact that technology is trending towards extremely high levels of integration at the package and chip levels, very high speeds of operation (> 100 GHz) and use of deeply scaled technology (approaching 10nm CMOS). In addition, a key test challenge will arise due to the ability to design complex systems such as robots that encompass sensors, communications systems, processors, transducers and enabling software. In addition to passing post-manufacture test procedures, such systems and relevant devices must exhibit fault-tolerance and survivability characteristics.

Topics of Interest (but are not limited to)

Original contributions in testing, fault tolerant and reliable computing are solicited. Topics of interest include, but are not limited to, the following categories:

Automatic Test Pattern Generation (ATPG)	Boundary Scan
Test Compression	Online Test
Temperature/Power-aware Test	Design-for-testability (DFT)
Microprocessor Test	Mixed signal and Analog Test
Memory Test	System-in-package (SiP)/ 3D Test
Test Quality and Reliability	Design Validation/Silicon Debug
Fault Modeling/Defect Based Test	Fault Simulation/Diagnosis
Software Testing	Board and System Test
Other	

Important Dates/Deadlines

Papers	~~May 27~~ June 10, 2011
Special Session proposals	~~June 3~~ June 17, 2011
Tutorial proposals	~~June 3~~ June 17, 2011
Exhibition/Booth proposals	~~May 27~~ June 10, 2011
Notification of acceptance	~~August 1~~ August 15, 2011
Camera-ready paper due date	~~August 22 September 5~~ September 20, 2011

Technical Co-Sponsors

Gold Sponsors

Silver Sponsors

	TRACK 1	TRACK 2	TRACK 3
DAY 1 (Sunday, Nov. 20)			
8:00AM-9:00AM	**REGISTRATION**		
9:00-10:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
10:30-11:00	**Tea Break**		
11:00-12:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
12:30-2:00	**Lunch Break**		
2:00-3:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
3:30-4:00	**Tea Break**		
4:00-5:30	**Tutorial Session** **- Tutorial 1: "Delay Test for High-Performance Designs"** **- Tutorial 2: "Scan Compression Techniques: Theory and Practice"**		
DAY 2 (Monday, Nov. 21)			
7:30AM-9:00AM	**REGISTRATION**		
9:00-11:00	**Plenary Session** **Inauguration** **General Chair's Address** **Program Chair's Address** **Plenary Keynote 1: Giovanni Demicheli, EPFL - "Nanosystems: devices, circuits, architectures and applications"** **Plenary Keynote 2: Janusz Rajski, Mentor Graphics - "The Future of Test – an EDA/DFT Perspective"**		
11:00 - 11:30	**Tea/Coffee Break**		
11:30 - 13:00	**Session A1: Testing Clock and Timing** ***Moderator: Pramod Notiyath, Synopsys*** 1. On Detecting Transition Faults in the Presence of Clock Delay Faults Yoshinobu Higami, Hiroshi Takahashi, Shin-Ya Kobayashi and Kewal Saluja 2. Testing of Clock-Domain Crossing Faults in Multi-Core System-on-Chip Naghmeh Karimi, Zhiqiu Kong, Krishnendu Chakrabarty, Pallav Gupta and Srinivas Patil 3. On-Chip Programmable Dual-Capture for Double Data Rate Interface Timing Test and Validation Hyunjin Kim and Jacob Abraham 4. Time Domain Characterization and Test of High Speed Signals Using Incoherrent Subsampling, Debesh Bhatta, Josh W Wells and Abhijit Chatterjee	**Session B1: Post-Silicon Debug and Validation** ***Moderator: Said Hamdioui, Delft Univ.*** 1. Post-Silicon Timing Validation Method using Path Delay Measurements Eun Jung Jang, Jaeyong Chung, Anne Gattiker, Sani Nassif and Jacob Abraham 2. Backward Reasoning with Formal Properties: A methodology for bug isolation on simulation traces Anvesh Komuravelli, Srobona Mitra, Ansuman Banerjee and Pallab Dasgupta 3. Design of a Test Processor for Asynchronous Chip Test Steffen Zeidler, Christoph Wolf, Milos Krstic, Frank Vater and Kraemer Rolf 4. On generating vectors for accurate post-silicon delay characterization Prasanjeet Das and Sandeep Gupta	**Special Session C1: Memory BIST Advances for Nanoscale Technologies** ***Organizer/Moderator: V. R. Devanathan, Texas Instruments*** **1. Physical-aware Memory BIST Datapath Synthesis: Architecture and Case -studies on Complex SoCs** **V. R. Devanathan, Sunil Bhavsar, Rajat Mehrotra (Texas Instruments)** **2. Failure Analysis and Test Solutions for Low-Power SRAMs** **L. B. Zordan, A. Bosio,, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel (LIRMM), N. Badereddine (Intel)** **3. A Robust Solution for Embedded Memory Test and Repair** **K. Darbinyan, G. Harutyunyan, S. Shoukourian, V. Vardanian, Y. Zorian (Synopsys)**
13:00 - 14:00	**Lunch Break**		
	Session A2: Power Aware Testing I		

14:00 - 15:30	***Moderator: Artur Pogiel, Mentor Graphics*** 1. Temperature Dependent Test Scheduling for Multi-core System-on-Chip Chunhua Yao, Kewal Saluja and Parameswaran Ramanathan 2. Test Scheduling for Multicore SoCs with Dynamic Voltage Scaling and Multiple Voltage Islands, Chrysovalantis Kavousianos, Krishnendu Chakrabarty, Arvind Jain and Rubin Parekhji 3. Selective Test Response Collection for Low-Power Scan Testing Dong Xiang 4. Low Power Test-Compression for High Test-Quality and Low Test-Data Volume Vasileios Tenentes and Chrysovalantis Kavousianos	**Session B2: Test Compression Techniques** ***Moderator: Tomoo Inoue, Hiroshima City U.*** 1. Predicting Scan Compression IP Configurations to Match the IP to the Design for Better QoR Rohit Kapur 2. Low Test Data Volume Low Power At-Speed Delay Tests Using Clock-Gating Elham Moghaddam, Janusz Rajski and Sudhakar Reddy 3. Test Compression Based on Lossy Image Encoding Hideyuki Ichihara, Yuka Iwamoto, Yuki Yoshikawa and Tomoo Inoue 4. Multiscan-based Test Data Compression Using UBI Dictionary and Bitmask Yang Yu, Gang Xiang and Liyan Qiao	**Special Session C2: Advanced Test Topics I** ***Moderator: Rajesh Gupta, Univ. of California (San Diego)*** **1: Memory technologies and test their test challenges Speaker: Manuel D'Abreu, Sandisk** **2: High Level Verification and its Use at Post-Silicon Debugging and Patching Speaker: Masahiro Fujita, Univ. of Tokyo**
15:30 - 16:00	**Tea/Coffee Break**		
16:00 - 17:30	**Session A3: Advanced Design for Testability Techniques** ***Moderator: Nagesh Tamarapalli, AMD*** 1. Multi-Cycle Test with Partial Observation on Scan-Based BIST Structure Yasuo Sato, Seiji Kajihara, Hiaso Yamaguchi and Makoto Matsuzono 2. SSTKR: Secure and Testable Scan Design Through Test Key Randomization Mohammed Abdul Razzaq, Virendra Singh and Adit Singh 3. An Innovative Methodology for Scan Chain Insertion and Analysis at RTL Lilia Zaourar, Yann Kieffer and Chouki Aktouf 4. Adaptation of Standard RT Level BIST Architectures to System Level Designs Nastaran Nemati and Zainalabedin Navabi	**Session B3: Advanced Techniques in Fault Diagnosis I** ***Moderator: Sandeep Gupta, Univ. of Southern California*** 1. Diagnostic Test of Robust Circuits Alejandro Cook, Sybille Hellebrand, Thomas Indlekofer and Hans-Joachim Wunderlich 2. An Accurate Timing-aware Diagnosis Algorithm for Multiple Small Delay Defects Po-Juei Chen, Wei-Li Hsu, James C.-M. Li, Nan-Hsin Tseng, Kuo-Yin Chen, Wei-Pin Changchien and Charles C. C. Liu 3. Diagnosis of Multiple Scan-Chain Faults in the Presence of System Logic Defects, Zhen Chen, Sharad Seth, Dong Xiang and Bhargab Bhattacharya 4. Diagnosing Multiple Slow Gates for Performance Tuning in the face of Extreme Process Variations, Xi Qian, Adit Singh and Abhijit Chatterjee	**Special Session C3: 3D Integrated Circuits: Design, Test, and Yield** ***Organizer/Moderator: Krishnendu Chakrabarty, Duke Univ.*** **1. Design of 3D-Specific Systems: Medium- and Long-Term Perspectives** **Paul Franzon (North Carolina State University)** **Speaker: Paul Franzon** **2. Testing and Design-for-Testability Techniques for 3D Integrated Circuits** **Brandon Noia and Krishnendu Chakrabarty (Duke University)** **Speaker: Krishnendu Chakrabarty** **3. Yield Improvement and Test Cost Optimization for 3D Stacked ICs** **Said Hamdioui (Delft University of Technology)** **Speaker: Said Hamdioui**
END OF DAY 2			
DAY 3 (Tuesday, Nov. 22)			
7:30AM-8:30AM	**REGISTRATION**		
8:30 - 9:15	**Distinguished Lecture 1:** **Rubin Parekhji, Texas Instruments - "Managing Test Cost and Test Quality on Large SOCs – Different Product Perspectives"** ***Moderator: Susmita Sur-Kolay, ISI***		
9:30 - 11:00	**Session A4: Power Aware Testing II** ***Moderator: Nilanjan Mukherjee, Mentor Graphics*** 1. Rewind-Support for Peak Capture Power Reduction in Launch-Off-Shift Testing Ozgur Sinanoglu 2. Low Power Decompressor and PRPG with Constant Value Broadcast Jerzy Tyszer, Michal Filipek, Yoshiaki Fukui, Hiroyuki Iwata, Grzegorz Mrugalski, Janusz Rajski and Masahiro Takakura 3. Effective Launch-to-Capture Power Reduction for LOS Scheme with Adjacent-Probability-Based X-Filling Kohei Miyase, Yuta Uchinodan, Kazunari Enokimoto, Yuta Yamato, Xiaoqing Wen, Seiji Kajihara, Fangmei Wu, Luigi Dilillo, Alberto Bosio, Patrick Girard and Arnaud Virazel 4. Virtual Circuit Model for Low Power Scan Testing in Linear Decompressor-based Compression	**Session B4: Test Quality Improvement Techniques** ***Moderator: Xiaowei Li, Institute of Computing Technology - CAS*** 1. A Process Monitor Based Speed Binning and Die Matching Algorithm Sreejit Chakravarty 2. Optimized Test Error Detection by Probabilistic Retest Recommendation Models Matthias Kirmse and Uwe Petersohn 3. Adaptive Test Framework for Achieving Target Test Quality at Minimal Cost Baris Arslan and Alex Orailoglu 4. A Fault Criticality Evaluation Framework of Digital Systems for Error Tolerant Video Applications, Yuntan Fang, Huawei Li and Xiaowei Li	**Special Session C4: Advanced Test Topics II** ***Moderator: Nicco (Shaleen) Bhabu, Cadence*** **1. Integrated Design & Test: Conquering the Conflicting Requirements of Low-Power, Variation-Tolerance, and Test Cost** **Ashish Goel, Swaroop Ghosh, Mesut Meterelliyoz (Purdue U) Jeff Parkhurst (Intel) and Kaushik Roy (Purdue U) Speaker: Kaushik Roy**

	Environment Zhen Chen, Jia Li, Dong Xiang and Yu Huang		
11:00 - 11:30	**Tea/Coffee Break**		
11:30 - 13:00	**Session A5: Defect Based Test Techniques** ***Moderator: Xiaoqing Wen, Kyushu Institute of Tech.*** 1. Test Pattern Selection for Defect-Aware Test Yoshinobu Higami, Hiroshi Furutani, Takao Sakai, Shuichi Kameyama and Hiroshi Takahashi 2. Efficient SAT-Based Search for Longest Sensitisable Paths Matthias Sauer, Jie Jiang, Alexander Czutro, Ilia Polian and Bernd Becker 3. Mapping Transaction Level Faults to Stuck-at Faults in Communication Hardware Fatemeh Javaheri, Majid Namaki-Shoushtari, Parastoo Kamranfar and Zainalabedin Navabi 4. On Generation of 1-Detect TDF Pattern Set with Significantly Increased SDD Coverage Fang Bao, Ke Peng, Krishnendu Chakrabarty and Mohammad Tehranipoor	**Session B5: Advanced Memory Test Techniques I** ***Moderator: Yasuo Sato, Kyushu Institute of Tech.*** 1. Efficient Use of Unused Spare Columns to Improve Memory Error Correcting Rate Umair Ishaq, Jihun Jung, Jaehoon Song and Sungju Park 2. New Fault Detection Algorithm for Multi-Level Cell Flash Memories Jaewon Cha, Ilwoong Kim and Sungho Kang 3. A New Test Paradigm for Semiconductor Memories in the Nano-Era Said Hamdioui, Venkataraman Krishnaswami, Ijeoma Sandra Irobi and Zaid Alars 4. On Defect Oriented Testing for Hybrid CMOS/memristor Memory Nor Zaidi Haron and Said Hamdioui	**Special Session C5: Robust Systems Research Around the Globe** ***Chair: Prof. Subhasish Mitra, Stanford University*** **1. Dependable VLSI Program in Japan: Program overview and the curent status of dependable VLSI platform project** **Prof. Hidetoshi Onodera (Kyoto U)** **2. Reliability: A Cross-Disciplinary and Cross-Layer Approach** **Prof. Norbert Wehn (University of Kaiserslautern)** **3. Underdesigned and Opportunistic Computing** **Prof. Puneet Gupta (UCLA) and Prof. Rajesh Gupta (UCSD)**
13:00 - 14:00	**Lunch Break**		
14:00 - 18:00PM	**SOCIAL PROGRAM**		
18:450-19:30PM	**Banquet Keynote: Sandeep Sinha (Lumis Partners)**		
19:30PM-20:00	**BANQUET AWARDS AND ANNOUNCEMENTS**		
20:00PM+	**BANQUET DINNER**		
DAY 4 (Wednesday, Nov. 23)			
7:30AM-8:30AM	**REGISTRATION**		
8:30 - 9:15	**Distinguished Lecture 2:** **Gordon Roberts, McGill University - "Time-Mode Signal Processing and Its Impact On Analog/Mixed-Signal/RF Testing"** ***Moderator: Adit Singh, Auburn U.***		
9:30 - 11:00	**Session A6: Advanced Techniques in Online Testing** ***Moderator: Kazumi Hatayama, Nara Institute of Science and Technology*** 1. Yield-per-area optimization for 6T-SRAMs using an integrated approach to exploit spares and ECC to efficiently combat high defect and soft-error rates Jae Chul Cha and Sandeep Gupta 2. A Hybrid Fault Tolerant Architecture for Robustness Improvement of Digital Circuits Duc Anh Tran, Arnaud Virazel, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch and Hans-Joachim Wunderlich 3. A new Architecture to Cross-Fertilize On-line and Manufacturing testing, Paolo Bernardi and Matteo Sonza Reorda 4. Online Test Macro Scheduling And Assignment In MPSoC Design Behnam Khodabandehloo, Seyed Alireza Hoseini, Sajjad Taheri, Mohammad Hashem Haghbayan, Mahmood Reza Babaei and Zeinolabedin Navabi	**Session B6: Advanced Techniques in RF/Mixed Signal Testing** ***Moderator: Michiko Inoue, Nara Institute of Science and Technology*** 1. Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs Manuel J. Barragan, Rafaella Fiorelli, Gildas Leger, Adoracion Rueda and Jose Luis Huertas 2. On Replacing an RF Test with an Alternative Measurement: Theory and a Case Study, Alexios Spyronasios, Louay Abdallah, Haralampos-G. Stratigopoulos and Salvador Mir 3. Test and Diagnosis of Analog Circuits using Moment Generating Functions Suraj Sindia, Vishwani Agrawal and Virendra Singh 4. Mixed-signal fault equivalence: search and evaluation Nuno Guerreiro and Marcelino Santos	**Special Session C6: Power-Aware Testing and Test of Low Power Designs** ***Organizer/Moderator: Patrick Girard, LIRMM*** **1. Power Aware Shift and Capture ATPG methodology for Low Power Designs** **S. Khullar, S. Bahl (STMicroelectronics)** **Speaker: S. Khullar** **2. Power-Aware Test Pattern Generation for At-Speed LOS Testing** **A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel (LIRMM), K. Miyase, X. Wen (Kyushu Institute of Technology)** **Speaker: A. Bosio** **3. Power Aware Embedded Test** **X. Lin, E. Moghaddam, N. Mukherjee B. Nadeau-Dostie, J. Rajski (Mentor Graphics), J. Tyszer (Poznan University of Technology)** **Speaker: N. Mukherjee**
11:00 - 11:30	**Tea/Coffee Break**		

11:30 - 13:00	**Session A7: Innovative Techniques in Microprocessor Testing** ***Moderator: Srikanth Venkataraman, Intel.*** 1. Distributed Comparison Test Driven Multiprocessor Speed-Tuning: Targeting Performance Gains Under Extreme Process Variations Jayaram Natarajan, Abhijit Chatterjee and Adit Singh 2. An Online Mechanism to Verify Datapath Execution using Existing Resources in Chip Multiprocessors, Rance Rodrigues and Sandip Kundu 3. An Efficient 2-Phase Strategy to Achieve High Branch Coverage Sarvesh Prabhu, Michael Hsiao, Saparya Krishnamoorthy, Loganathan Lingappan, Vijay Gangaram and Jim Grundy 4. Soft error recovery technique for multiprocessor SOPC Uroš Legat, Anton Biasizzo and Franc Novak	**Session B7: Test Automation and Analysis** ***Moderator: Subhasish Mukherjee (Cadence)*** 1. Efficient BDD-based Fault Simulation in Presence of Unknown Values Michael Kochte, Sandip Kundu, Kohei Miyase, Xiaoqing Wen and H.-J. Wunderlich 2. Analysis of Resistive Bridge Defect Delay Behavior in the Presence of Process Variation Shida Zhong, Saqib Khursheed, Bashir Al-Hashimi, Sudhakar Reddy and Krishnendu Chakrabarty 3. Automation of 3D DfT Insertion, Sergej Deutsch, Vivek Chickermane, Brion Keller, Subhasish Mukherjee, Mario Konijnenburg, Erik Jan Marinissen and Sandeep K. Goel 4. MarciaTesta: an EDA tool for the automatic generator of test program for microprocessor data caches, Marco Indaco	**Special Session C7: Post-Si Debug and Validation** ***Moderator: Rubin Parekhji, Texas Instruments*** **Invited Talk 1. Sneak peek at growing HVM Test and Debug challenges associated with Ring Architecture based Intel® Xeon® Processor Speaker: Shridhar Bendi, Intel** **Invited Talk 2. Structured Silicon Debug: Key for Reducing Time to Production Speaker: Srinivas Vooka, Texas Instruments**
13:00 - 14:00	**Lunch Break**		
14:00 - 15:30	**Session A8: 3D IC Testing** ***Moderator: Indranil Sengupta, IIT - Kharagpur*** 1. Wrapper Chain Design for Testing TSVs Minimization in Circuit-Partitioned 3D SoC Yuanqing Cheng, Lei Zhang, Yinhe Han, Jun Liu and Xiaowei Li 2. Identification of Defective TSVs in Pre-Bond Testing of 3D ICs Brandon Noia and Krishnendu Chakrabarty 3. A Unified Interconnects Testing Scheme for 3D Integrated Circuits Chih-Yun Pai, Liang-Bi Chen, Bo-Chuan Cheng, Jie-Chi Chen, Katherine Shu-Min Li and Ji-Jan Chen 4. Cost-Effective TSV Grouping for Yield Improvement of 3D-ICs Yi Zhao, Saqib Khursheed and Bashir Al-Hashimi	**Session B8: Advanced Memory Test Techniques II** ***Moderator: Seiji Kajihara, Kyushu Institute of Technology*** 1. Test for Parasitic Memory Effect in SRAMs Ijeoma Sandra Irobi, Zaid Alars, Said Hamdioui and Claude Thibeault 2. Transient Noise Failures in SRAM Cells: Dynamic Noise Margin Metric Elena Ioana Vatajelu, Álvaro Gómez-Pau, Michel Renovell and Joan Figueras 3. Fault Diagnosis in Memory BIST Environment with Non-March Tests Jerzy Tyszer, Grzegorz Mrugalski, Artur Pogiel, Nilanjan Mukherjee, Janusz Rajski and Pawel Urbanek 4. Characterizing Pattern Dependent Delay Effects in DDR Memory Interfaces, Atul Gupta, Ajay Kumar and Manas Chhabra	**Special Session C8: Embedded Tutorial - Testability of Cryptographic Hardware and Detection of Hardware Trojans** ***Moderator: Jacob Abraham, University of Texas, Austin*** **Speakers: Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, IIT Kharagpur**
15:30 - 16:00	**Tea/Coffee Break**		
16:00 - 17:30	**Session A9: Advanced Techniques in Fault Diagnosis II** ***Moderator: Huawei Li, Institute of Computing Technology*** 1. Improved Fault Diagnosis for Reversible Circuits Hongyan Zhang, Robert Wille and Rolf Drechsler 2. Embedded Test for Highly Accurate Defect Localization, Abdullah Mumtaz, Michael E. Imhof, Stefan Holst and Hans-Joachim Wunderlich 3. On Using Design Partitioning To Reduce Diagnosis Memory Footprint Xiaoxin Fan, Huaxing Tang, Sudhakar M. Reddy, Wu-Tung Cheng and Brady Benware 4. Exploring Impact of Faults on Branch Predictors' Power for Diagnosis of Faulty Module, Gunjan Bhattacharya, Ilora Maity, Baisakhi Das and Biplab K Sikdar	**Session B9: Innovative DFT Solutions** ***Moderator: Kenneth Pichamuthu, IBM*** 1. Breaking the Test Application Time Barriers in Compression: Adaptive Scan – Cyclical (AS-C) Anshuman Chandra, Jyotirmoy Saikia and Rohit Kapur 2. Exploiting Free LUT Entries to Mitigate Soft Errors in SRAM-based FPGAs Keheng Huang, Yu Hu and Xiaowei Li 3. A Single-Configuration Method for Application-Dependent Testing of SRAM-based FPGA Interconnects Thulasiraman Nandhakumar, Haider Almurib and Fabrizio Lombardi 4. Multi-Visit TAMs to Reduce the Post-Bond Test Length of 2.5D-SICs with a Passive Silicon Interposer Base Chun-Chuan Chi, Erik Jan Marinissen, Sandeep Kumar Goel and Cheng-Wen Wu	**Session C9: Board and System Level Testing** ***Moderator: Erik Larsson, Linkoping University*** 1. Test Scheduling in an IEEE P1687 Environment with Resource and Power Constraints Farrokh Ghani Zadegan, Urban Ingelsson, Golnaz Asani, Gunnar Carlsson and Erik Larsson 2. Automatic SoC Level Test Path Synthesis Based on Partial Functional Models Anton Tsertov, Artur Jutman, Sergei Devadze and Raimund Ubar 3. A Boundary Scan Circuit with Time-to-Digital Converter for Delay Testing Hiroyuki Yotsuyanagi, Hiroyuki Makimoto and Masaki Hashizume 4. Burst-Mode Transmission and Data Recovery for Multi-GHz Optical Packet Switching Network Testing Carl Gray, David Keezer, Howard Wang and Keren Bergman

Tutorial Sessions will be held at the same venue, on Sunday, November 20, 2011.

Tutorial 1: Delay Test for High-Performance Designs

Srinivas Patil, *Intel Corporation(USA)* and Sreejit Chakravarty, *LSI Corporation(USA)*

Tutorial Summary:

Today's nanometer designs continue pushing the performance envelope under the constraints of power and area. The combination of smaller design margins, and the inherent process variability requires addressing defects beyond static defects, particularly delay defects. The goal of this tutorial is to address testing for delay defects in a comprehensive yet practical fashion. The tutorial will start with a general introduction to delay defects, followed by a discussion of various fault models used to model them. This will be followed by a discussion of various testing techniques needed to target delay faults, including the DFT support needed in the design. We will discuss various techniques needed to improve the efficacy of delay testing, including metrics beyond gross fault coverage to measure their effectiveness, inclusion of timing information to target critical paths, accounting of environmental conditions such as cross-talk and power droop, utilization of hardware compression techniques to reduce delay test cost, and diagnosis techniques needed to pin-point delay test failures for failure analysis and yield enhancement. Throughout the tutorial, we will use real-world examples of delay test implementation based upon representative industrial test cases. Though the tutorial focus is on the concepts behind delay testing rather than particular EDA tools which enable automation, we will mention generic tool capabilities where appropriate.

The intended audience for this tutorial is practicing engineers (Design, DFT, Product Test, Reliability, Design Automation), Design and DFT Managers, students and academicians. The goal is to leverage from more than 25 years research and industrial practice in the delay test area, to present an overview of theoretical and practical aspects of delay test. At the end of this tutorial, the attendees should be able to gain a broad overview of this area, along with an understanding of relevance and applicability to their own environment. There are no pre-requisites for this tutorial: the tutorial will build from the basics to advanced concepts, and will be appropriate for those who are new to this area, as well as those who want to delve into the more advanced concepts of delay testing and fine-tune their existing methodology.

Tutorial 2: Scan Compression Techniques: Theory and Practice

Rohit Kapur, *Synopsys, Inc.(USA)*; Nagesh Tamarapalli, *AMD (India)*; Arvind Jain, *Texas Instruments (India)* and Rubin Parekhji, *Texas Instruments (India)*

Tutorial Summary:

Large designs, larger test pattern volumes and longer test times have necessitated the use of test data volume and test time compression techniques built around the scan design paradigm. The adoption of these techniques is increasing. Much as well as they are understood today, these techniques continue to present challenges in their adoption and implementation. As their adoption increases, new compression targets are set, in turn forcing the investigation of better solutions and upper bounds.

This tutorial will provide a comprehensive coverage of scan compression. It will begin with cost models to help designers understand the choices available to them. Mathematical formulations for different compression techniques and their influence on test pattern generation will be presented. Implementation techniques and tradeoffs will be described through various examples derived from IP (intellectual property) cores and large chips. Diagnostics, which is an important part of deep sub-micron designs, will also be discussed within the realm of compression, together with techniques which improve diagnosability. Emerging developments in this technology will be described. Finally, compression results from case studies involving different flavours of IPs and SOCs will be presented to illustrate how best the theory and practice fit together.

The attendees will appreciate the nuances of scan compression, various tradeoffs in their adoption, and entitlement gaps better, and gather additional insight into what promises can be made in terms of practical bounds, compression friendly designs, the (non-)tolerance to Xs, and pattern optimisations. They will also appreciate from the implementation viewpoint the duality between test data volume and test time (test cycles), modular compression architectures for large SOCs (system-on-chips), and the design space between traditional ATPG and classical logic BIST.

Technical Co-Sponsors

Gold Sponsors

Silver Sponsors

ATS 2011 Organizing Committee| ats2011_orgcomittee@yahoogroups.com

Selected papers in ATS 20th Anniversary Compendium of Papers

ATS 2002

Integrated Test Scheduling, Test Parallelization and TAM Design
Erik Larsson, Klas Arvidsson, Hideo Fujiwara and Zebo Peng

On Generating High Quality Tests for Transition Faults
Yun Shao, Irith Pomeranz and Sudhakar M. Reddy

A Scheduling Method in High-Level Synthesis for Acyclic Partial Scan Design
Tomoo Inoue, Tomokazu Miura, Akio Tamura, and Hideo Fujiwara

Test Scheduling and Test Access Architecture Optimization for System-on-Chips
Huan-Shan Hsu, Jing-Reng Huang, Kuo-Liang Cheng, Chih-Wea Wang

Test Scheduling of BISTed Memory Cores for SOC
Chih-Wea Wang, Jing-Reng Huang, Yen-Fu Lin, Kuo-Liang Cheng, Chih-Tsun Huang, and Chen-Wen Wu

A Concurrent Fault Simulation for Crosstalk Faults in Sequential Circuit
Marong Phadoongsidhi, Kim T. Le, and Kewal K. Saluja

ATS 2003

Test Resource Partitioning Based on Efficient Response Compaction for Test Time and Tester Channels Reduction
Yinhe Han, Yongjun Xu, Huawei Li, Xiaowei Li and Ashuman Chandra

Optimal Scan Tree Construction with Test Vector Modification for Test Compression
Kohei Miyase and Seiji Kajihara

A Processor-Based Built-In Self-Repair Design for Embedded Memories
Chin-Lung. Su, Rei-Fu Huang, andCheng-Wen Wu

Test Synthesis for Datapaths Using Datapath-Controller Functions
Michiko Inoue, Kazuhiro Suzuki, Hiroyuki Okamoto, and Hideo Fujiwara

Test Data Manipulation Techniques for Energy-Frugal, Rapid Scan Test
Ozgur Sinanoglu and Alex Orailoglu

Efficient Diagnosis for Multiple Intermittent Scan Chain Hold-Time Faults
Yu Huang, Wu-Tung Cheng, Cheng-Ju Hsieh, Huan-Yung Tseng, Alou Huang, and Yu-Ting Hung

ATS 2004

Compactor Independent Direct Diagnosis
Wu-Tung Cheng, Kun-Han Tsai, Yu Huang, Nagesh Tamarapalli, and Janusz Rajski

Test Power Reduction with Multiple Capture Orders
Kuen-Jong Lee, Shaing-Jer Hsu, and Chia-Ming Ho

Testing for Missing-Gate Faults in Reversible Circuits
John P. Hayes, Ilia Polian, and Bernd Becker

Intelligible test techniques to support error-tolerance
Melvin Breuer

Multiple Scan Tree Design with Test Vector Modification
Kohei Miyase, Seiji Kajihara, and Sudhakar M. Reddy

High Level Fault Injection for Attack Simulation in Smart Cards
K. Rothbart, U. Neffe, C. Steger, R. Weiss, E. Rieger, and A. Mühlberger

ATS 2005

Untestable multi-cycle path delay faults in industrial designs
Manan Syal, Michael S. Hsiao, Surlyaprakash Natarajan, and Sreejit Chakravarty

A DFT method for RTL data paths based on partially strong testability to guarantee complete fault efficiency
Hiroyuki Iwata, Tomokazu Yoneda, Satoshi Ohtake, and Hideo Fujiwara

Shannon expansion based supply-gated logic for improved power and testability
S. Ghosh, S. Bhunia, and K. Roy

Robust built-in test of RF ICs using envelope detectors
Donghoon Han and Abhijit Chatterjee

Bridge defect diagnosis with physical information
Wei Zou,Wu-Tung Cheng, and Sudhakar M. Reddy

Chip identification using the characteristic dispersion of transistor
Junichi Hirase and Tatsuya Furukawa

ATS 2006

Timing-Aware ATPG for High Quality At-speed Testing of Small Delay Defects
Xijiang Lin, Kun-Han Tsai, Chen Wang, Mark Kassab, Janusz Rajski, Takeo Kobayashi, Randy Klingenberg, Yasuo Sato, Shuji Hamada, and Takashi Aikyo

Interconnect Open Defect Diagnosis with Physical Information
Wei Zou, Wu-Tung Cheng, and Sudhakar Reddy

A Scan Chain Adjustment Technology for Test Power Reduction
Jia Li, Yu Hu, and Xiaowei Li

Power-Aware Test Data Compression for Embedded IP Cores
Nabil Badereddine, Zhanglei Wang, Patrick Girard, Krishnendu Chakrabarty, Arnaud Virazel, Serge Pravossoudovitch, and Christian Landrault

An External Test Approach for Network-on-a-Chip Switches
Jaan Raik, Vineeth Govind, and Raimund Ubar

An Efficient Test Pattern Selection Method for Improving Defect Coverage with Reduced Test Data Volume and Test Application Time
Zhanglei Wang and Krishnendu Chakrabarty

ATS 2007

An Accurate Jitter Estimation Technique for Efficient High Speed I/O Testing
Dongwoo Hong and Kwang-Ting (Tim) Cheng

An On-Chip Test Clock Control Scheme for Multi-Clock At-Speed Testing
Xiao-Xin Fan, Yu Hu, and Laung-Terng (L. -T.). Wang

Improving Test Pattern Compactness in SAT-Based ATPG
Stephan Eggersglub and Rolf Drechsler

Improving Circuit Robustness with Cost-Effective Soft-Error-Tolerant Sequential Elements
Mingjing Chen and Alex Orailoglu

Flip-flop Selection to Maximize TDF Coverage with Partial Enhanced Scan
Gefu Xu, Adit D. Singh

Clues for Modeling and Diagnosing Open Faults with Considering Adjacent Lines
Hiroshi Takahashi, Yoshinobu Higami, Shuhei Kadoyama, Takashi Aikyo, and Yuzo Takamatsu

ATS 2008

Test Power Reduction by Blocking Scan Cell Outputs
Xijiang Lin and Janusz Rajski

Low-Cost One-Port Approach for Testing Integrated RF Substrates
Abhilash Goyal and Madhavan Swaminathan

Interconnect-Driven Layout-Aware Multiple Scan Tree Synthesis for Test Time, Data Compression and Routing Optimization
Katherine Shu-Min Li, and Jr-Yang Huang

Untestable Fault Identification in Sequential Circuits Using Model-Checking
Jaan Raik, Hideo Fujiwara, Raimund Ubar, and Anna Krivenko

A Test Generation Method for State-Observable FSMs to Increase Defect Coverage under the Test Length Constraint
Ryoichi Inoue, Toshinori Hosokawa, and Hideo Fujiwara

A Re-design Technique of Datapath Modules in Error Tolerant Application
Doochul Shin and Sandeep K. Gupta

ATS 2009

A Non-intrusive and Accurate Inspection Method for Segment Delay Variabilities
Ying-Yen Chen and Jing-Jia Liou

CAT: A Critical-Area-Targeted Test Set Modification Scheme for Reducing Launch Switching Activity in At-Speed Scan Testing
K. Enokimoto, X. Wen, Y. Yamato, K. Miyase, H. Sone, S. Kajihara, M. Aso, and H. Furukawa

BIST Driven Power Conscious Post-Manufacture Tuning of Wireless Transceiver Systems Using Hardware-Iterated Gradient Search
Vishwanath Natarajan, Shyam Kumar Devarakond, Shreyas Sen, and Abhijit Chatterjee

A Practical Approach to Threshold Test Generation for Error Tolerant Circuits
Hideyuki Ichihara, Kenta Sutoh, Yuki Yoshikawa, and Tomoo Inoue

M-IVC: Using Multiple Input Vectors to Minimize Aging-induced Delay
Song Jin, Yinhe Han, Lei Zhang, Huawei Li, Xiaowei Li, and Guihai Yan

An On-Chip Integrator Leakage Characterization Technique and Its Application to Switched Capacitor Circuits Testing
Chen-Yuan Yang, Xuan-Lun Huang, and Jiun-Lang Huang

ATS 2010

Tackling the Path Explosion Problem in Symbolic Execution-driven Test Generation
Saparya Krishnamoorthy, Michael Hsiao, and Loganathan Lingappan

Rapid Radio Frequency Amplitude and Phase Distortion Measurement Using Single-tone AM Stimulus
Shreyas Sen, Shyam Devarakond, and Abhijit Chatterjee

Variation-Aware Fault Modeling
Fabian Hopsch, Bernd Becker, Sybille Hellebrand, Ilia Polian, Bernd Straube

Diagnosis of Multiple Physical Defects Using Logic Fault Models
Xun Tang, Wu-Tung Cheng, Ruifeng Guo, and Sudhakar Reddy
Power-Safe Application of Transition Delay Fault Patterns Considering Current Limit during Wafer Test
Wei Zhao, Junxia Ma, Mohammad Tehranipoor, and Sreejit Chakravarty
Circuit Topology-Based Test Pattern Generation for Small-Delay Defects
Sandeep Kumar Goel, Krishnendu Chakrabarty, Mahmut Yilmaz, Ke Peng, and Mohammad Tehranipoor

ATS 2011
Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs
Manuel J. Barragan, Rafaella Fiorelli, Gildas Leger, Adoracion Rueda and Jose Luis Huertas
Fault Diagnosis in Memory BIST Environment with Non-March Tests
Jerzy Tyszer, Grzegorz Mrugalski, Artur Pogiel, Nilanjan Mukherjee, Janusz Rajski and Pawel Urbanek
Diagnosing Multiple Slow Gates for Performance Tuning in the face of Extreme Process Variations
Xi Qian, Adit Singh and Abhijit Chatterjee
Post-Silicon Timing Validation Method using Path Delay Measurements
Eun Jung Jang, Jaeyong Chung, Anne Gattiker, Sani Nassif and Jacob Abraham
An Efficient 2-Phase Strategy to Achieve High Branch Coverage
Sarvesh Prabhu, Michael Hsiao, Saparya Krishnamoorthy, Loganathan Lingappan, Vijay Gangaram and Jim Grundy
Efficient BDD-based Fault Simulation in Presence of Unknown Values
Michael Kochte, Sandip Kundu, Kohei Miyase, Xiaoqing Wen and H.-J. Wunderlich
Characterizing Pattern Dependent Delay Effects in DDR Memory Interfaces
Atul Gupta, Ajay Kumar and Manas Chhabra

Selected papers in ATS 10th Anniversary Compendium of Papers

ATS 1992

An Approach to Design-for-Testability for Memory Embedded Logic LSIs
K.Hatayama, T.Hayashi, M.Takakura, T.Suzuki, S.Michishita, and H.Satoh

Synthesis for Testability of PLA Based Finite State Machines
M.J.Avedillo, J.M.Quintana and J.L.Huertas

A Concurrent Fault Detection Method for Superscalar Processors
A. P. Pawlovsky and M. Hanawa

A Method of Diagnosing Logical Faults in Combinational Circuits
K.Yamazaki and T.Yamada

Reduction of Dynamic Memory Usage in Concurrent Fault Simulation for Synchronous Sequential Circuits
K.Kim and K.K.Saluja

ATS 1993

Test Set Partitioning and Dynamic Fault Dictionary for Sequential Circuits
P.G.Ryan and W.K Fuchs

A Two-Phase Fault-Simulation Scheme for Sequential Circuits
W- C. Wu, C-L.n Lee, and J- E. Chen

GID--Testable Two-Dimensional Sequential Arrays for Self-Testing
W.K.Huang, F.Lombardi, and M.Lu

A Global BIST Methodology
T.Gheewala, H.Sucar, and P.Varma

On Properties and Implementations of Inverting ALSC for Use in Built-In Self-Testing
K Furuya, P.Y.Koh, and E.J.McCluskey

ATS 1994

Efficient Test Sequence Generation for Localization of Multiple Faults in Communication Protocols
Y. Kakuda, H. Yukitomo, S. Kusumoto, and T. Kikuno

Design of Random Pattern Testable Floating Point Adders
J. Rajski and J. Tyszer

Testability Considerations in Technology Mapping
I. Pomeranz and S. M. Reddy

Analysis and Improvement of Testability Measure Approximation Algorithms
J. Bitner, J. Jain, J.A. Abraham, and D.S. Fussell

Efficiency Improvements for Multiple Fault Diagnosis of Combinational Circuits
N. Yanagida, H. Takahashi, and Y. Takamatsu

Boolean Process - An Analytical Approach to Circuit Representation
Y.Min

ATS 1995

Software Transformations for Sequential Test Generation
A. Balakrishnan and S. T. Chakradhar

DC Control and Observation Structures for Analog Circuits
Y-R. Shieh and C. W. Wu

Universal Test Complexity of Field-Programmable Gate Arrays
T. Inoue, H. Fujiwara, H. Michinishi, T. Yokohira, and T. Okamoto
A Design-for-Test Technique for Multi-Stage Analog Circuits
M. Renovell, F. Azais, and Y. Bertrand
Fanout Fault Analysis for Digital Logic Circuits
J. E. Chen, C. L. Lee, W. Z. Shen, and B. Chen
Theory and Applications of Cellular Automata for Synthesis of Easily Testable Combinational Logic
S. Nandi and P. Pal Chaudhuri
Low Power Design and Its Testability
H. Ueda and K. Kinoshita

ATS 1996
Redundancy Identification Using Transitive Closure
V.D. Agrawal, M.L. Bushnell, and Q. Lin
A Consistent Scan Design System for Large-Scale ASICs.
Y. Konno, K. Nakamura, T. Bitoh, K. Saga, and S. Yano
Combination of Automatic Test Pattern Generation and Built-In Intermediate Voltage Sensing for Detecting CMOS Bridging Faults
K.-J. Lee, J.-J. Tang, T.-C. Huang, and C.-L. Tsai
Partially Parallel Scan Chain for Test Length Reduction by Using Retiming Technique
Y. Higami, S. Kajihara, and K. Kinoshita
An Efficient Compact Test Generator for IDDQ Testing
H. Kondo and K.-T. Cheng

ATS 1997
FaultMaxx: A Perturbation Based Fault Modeling and Simulation for Mixed-Signal Circuits
N. Ben-Hamida, K. Saab, D. Marche, and B. Kaminska
On the Complexity of Universal Fault Diagnosis for Look-up Table FPGAs
T. Inoue, S. Miyazaki, and H. Fujiwara
Testing for the Programming Circuit of LUT-based FPGAs
H. Michinishi, T. Yokohira, T. Okamoto, T. Inoue, and H. Fujiwara
Test Length for Random Testing of Sequential Machines Application to RAMs
R. David
A Genetic Algorithm for Computation of Initialization Sequences for Synchronous Sequential Circuits
F. Corno, P. Prinetto, M. Rebaudengo, M. S. Reorda, and G. Squillero
On Chip Weighted Random Patterns
J. Savir

ATS 1998
Vector Restoration Using Accelerated Validation and Refinement.
S.K. Bommu, S.T. Chakradhar, and K.B. Doreswamy
March LA: A Test for All Linked Memory Faults
A.J. van de Goor, G.N. Gaydadjiev, V.N. Yarmolik, and V.G. Mikitjuk
Test Cycle Count Reduction in a Parallel Scan BIST Environment

B.Ayari and P. Varma

BIST TPG for Combinational Cluster (Glue Logic) Interconnect Testing at Board Level

C.-H. Chiang and S.K. Gupta

False-Path Removal Using Delay Fault Simulation

M.A. Gharaybeh, V.D. Agrawal, and M.L. Bushnell

A Ring Architecture Strategy for BIST Test Pattern Generation

C. Fagot, O. Gascuel, P. Girard, and C. Landrault

ATS 1999

High Resolution CD-SEM System

Y. Ose, M. Ezumi, and H. Todokoro

An Evaluation of Test Generation Algorithms for Combinational Circuits

S. Xu and T. J. Frank

An Effective Methodology for Mixed Scan and Reset Design Based on Test Generation and Structure of Sequential Circuits

H-C. Liang and C. L. Lee

Circuit Partitioning for Low Power BIST Design with Minimized Peak Power Consumption

P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch

New DFT Techniques of Non-Scan Sequential Circuits with Complete Fault Efficiency

D. K. Das, S. Ohtake, and H. Fujiwara

ATS 2000

Test Generation for Crosstalk-Induced Faults: Framework and Computational Results

W-Y. Chen, S. Gupta, and M. Breuer

A Class of Sequential Circuits with Combinational Test Generation Complexity under Single-Fault Assumption

M. Inoue, E. Gizdarski, and H. Fujiwara

Fast Hierarchical Test Path Construction for DFT-free Controller-Datapath Circuits

Y. Makris, J. Collins, and A. Orailoglu

A New Framework for Static Timing Analysis, Incremental Timing Refinement, and Timing Simulation

L-C. Chen, S. K. Gupta, and M. A. Breuer

Accelerated Test Pattern Generators for Mixed-Mode BIST Environments

W-L. Wang and K-J. Lee

ATS 2001

Short Circuit Faults in State-Of-The-Art ADC's - Are They Hard or Soft?

A. Lechner, A. M. D. Richardson and B. Hermes

EB-Testing-Pad Method and its Evaluation by Actual Devices

N. Kuji and T. Ishihara

Robust Concurrent Self Test of Linear Digital Systems

E. Simeu, A. Abdelhay, and M. A. Naal

Resource Allocation and Test Scheduling for Concurrent Test of Core-Based SOC Design

20TH ANNIVERSARY COMPENDIUM OF PAPERS FROM ASIAN TEST SYMPOSIUM

ATS 20th Anniversary Compendium Editorial Committee

Chair: Hideo Fujiwara, *Osaka Gakuin University*
Vice-Chair: Virendra Singh, *Indian Institute of Science*
Members:
Kiyoshi Furuya, *Chuo University (ATS 2002 PC Chair)*
Xiaowei Li, *Chinese Academy of Sciences (ATS 2003 PC Co-chair)*
Masaki Hashizume, *University of Tokushima (ATS 2003 PC Co-chair)*
Shi-Yu Huang,, *National Tsing-Hua University (ATS 2004 PC Co-chair)*
Ming-Der Shieh, *National Cheng-Kung University (ATS 2004 PC Co-chair)*
Krishnendu Chakrabarty, *Duke University (ATS 2005 PC Co-chair)*
Dipanwita Roy Chowdhury, *Indian Institute of Technology, Kharagpur (ATS 2005 PC Co-chair)*
Seiji Kajihara, *Kyushu Institute of Technology (ATS 2006 PC Chair)*
Huawei Li, *Chinese Academy of Sciences (ATS 2007 PC Co-chair)*
Xiaoqing Wen, *Kyushu Institute of Technology (ATS 2007 PC Co-chair)*
Kazumi Hatayama, *Nara Institute of Science and Technology (ATS 2008 PC Co-chair)*
Hiroshi Takahashi, *Ehime University (ATS 2008 PC Vice-chair)*
Sying-Jyan Wang, *National Chung Hsing University (ATS 2009 PC Chair)*
Jianhua Gao, *Shanghai Normal University (ATS 2010 PC Co-chair)*
Yasuo Sato, *Kyushu Institute of Technology (ATS 2010 PC Co-chair)*
Sandip Kundu, *University of Massachusetts, Amherst (ATS 2011 PC Co-chair)*
Srivaths Ravi, *Texas Instruments (ATS 2011 PC Co-chair)*
Finance: Virendra Singh, *Indian Institute of Science*
Gulshan Dua, *Freescale Semiconductor, Noida*
Publications: S. Sur-Kolay, *ISI, Kolkata, India*
Michiko Inoue, *Nara Institute of Science and Technology*

ATS 2002 - 2011 for the second decade

Eleventh Asian Test Symposium, November 18-20, 2002, Guam, USA
Twelfth Asian Test Symposium, November 16-19, 2003, Xi'an, China
Thirteenth Asian Test Symposium, November 15-17, 2004, Kenting, Taiwan
Fourteenth Asian Test Symposium, December 18-21, 2005, Kolkata, India
Fifteenth Asian Test Symposium, November 20-23, 2006, Fukuoka, Japan
Sixteenth Asian Test Symposium, October 9-11, 2007, Beijing, China
Seventeenth Asian Test Symposium, November 24-27, 2008, Sapporo, Japan
Eighteenth Asian Test Symposium, November 23-26, 2009, Taichung, Taiwan
Nineteenth Asian Test Symposium, December 1-4, 2010, Shanghai, China
Twentieth Asian Test Symposium, November 21-23, 2011, New Delhi, India

10TH ANNIVERSARY COMPENDIUM OF PAPERS FROM ASIAN TEST SYMPOSIUM

ATS 10th Anniversary Compendium Editorial Committee

Chair: Hideo Fujiwara, *Nara Institute of Science and Technology (ATS 1992 PC Chair)*

Members:

Yinghua Min, *Chinese Academy of Science (ATS 1993 PC Chair)*

Yuzo Takamatsu, *Ehime University (ATS 1994 PC Chair)*

Vishwani D. Agrawal, *AT&T Bell Laboratories (ATS 1995 PC Chair)*

Cheng-Wen Wu, *National Chiao Tung University (ATS 1996 PC Chair)*

Serge Demidenko, *Singapore Polytechnic (ATS 1998 PC Co-chair)*

Kiyoshi Furuya, *Chuo University (ATS 1998 PC Co-chair)*

Shiyi Xu, *Shanghai University (ATS 1999 PC Chair)*

Kuen-Jong Lee, *National Cheng Kung University (ATS 2000 PC Co-chair)*

Chau-Chin Su, *National Central University (ATS 2000 PC Co-chair)*

Hiromi Hiraishi, *Kyoto Sangyo University (ATS 2001 PC Chair)*

Kazumi Hatayama, *Hitachi Ltd. (ATS 2001 PC Vice-chair)*

Secretary: Michiko Inoue, *Nara Institute of Science and Technology*

* ATS 1997 PC Chair, Teruhiko Yamada, was not included owing to his eternal sleep.

ATS 1992 - 2001 for the first decade

First Asian Test Symposium, November 26-27, 1992, Hiroshima, Japan
Second Asian Test Symposium, November 16-18, 1993, Beijing, China
Third Asian Test Symposium, November 15-17, 1994, Nara, Japan
Fourth Asian Test Symposium, November 23-24, 1995, Bangalore, India
Fifth Asian Test Symposium, November 20-22, 1996, Hsinchu, Taiwan
Sixth Asian Test Symposium, November 17-19, 1997, Akita, Japan
Seventh Asian Test Symposium, December 2 - 4, 1998, Singapore
Eighth Asian Test Symposium, November 16-18, 1999, Shanghai, China
Ninth Asian Test Symposium, December 4-6, 2000, Taipei, Taiwan
Tenth Asian Test Symposium, November 19-21, 2001, Kyoto, Japan