The Asian Test Symposium (ATS) provides an open forum for researchers and engineers from all countries of the world, especially from Asia, to exchange innovative ideas on system, board, and device testing with design, manufacturing and field considerations in mind. The official language of the symposium is English.

Scopes

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- Automatic Test Generation / Fault Simulation
- Design for Testability / DfX
- Built-In Self-Test
- Test Data Compression
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- Design Verification
- Low-power Testing
- Defect-Based Testing / IDDX Testing
- Fault Modeling & Diagnosis
- Memory Test / FPGA Test
- Analog and Mixed-Signal Test
- RF Testing
- High-Speed I/O Test
- System-on-a-Chip Test
- System-in-Package Test
- Board and System Test
- On-line Testing
- Network Protocol Testing / NoC Testing
- Software Testing
- Economics of Test

Key Dates

Submission deadline: May 18, 2009
Notification of acceptance: July 10, 2009
Camera-ready copy: August 10, 2009
Symposium: November 23-26, 2009

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Industrial Session Deadline Extended to July 6, 2009

Submission deadline: July 6, 2009
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Submission Deadline Extended to May 18, 2009

May 18: Deadline for regular paper submission.
May 23: Deadline for revisions of submitted papers.

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Taiwan Institute of Electrical and Electronics Engineering

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Program at a Glance

Date	Time	Program		
Nov. 23 (Mon.)	09:00-12:00	Tutorial 1		
	14:00-17:00	Tutorial 2		
	18:30-21:00	Welcome Reception		
Nov. 24 (Tue.)	09:00-10:20	Plenary Session 1		
	10:20-10:40	Coffee Break		
	10:40-12:00	Plenary Session 2		
	12:00-13:10	Lunch		
	13:10-14:30	3A: BIST	3B: Fault Diagnosis	3C: Analog and Mixed-signal Testing
	14:30-14:45	Coffee Break		
	14:45-16:05	4A: Industrial Session	4B: Low-Power Testing	4C: On-Line Testing and Silicon Debug
	16:05-16:20	Coffee Break		
	16:20-17:40	5A: Delay Testing	5B: Test Generation (I)	5C: System Test
Nov. 25 (Wed.)	09:00-10:20	6A: Panel Session (I)	6B: DFT	6C: RF and Analog Testing
	10:20-10:40	Coffee Break		
	10:40-12:00	7A: SoC Test	7B: Test Generation (II)	7C: Test Data Compression
	12:00-13:30	Lunch		
	13:30-18:30	Social Event		
	18:30-20:00	Banquet		
Nov. 26 (Thu.)	09:00-10:20	8A: Panel Session (II)	8B: Fault Modeling & Diagnosis	8C: Analog and Mixed-signal Testing
	10:20-10:40	Coffee Break		
	10:40-12:00	9A: Memory Test	9B: Test Generation (III)	9C: Defect-Based Testing

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Advance Program:

Nov. 23, 2009

9:00-12:00 Tutorial 1
Power-Aware Testing and Test Strategies for Low Power Devices

13:30-16:30 Tutorial 2
System-in-Package Test Strategies

Nov. 24, 2009

9:00-10:30 Plenary Session 1

9:00-9:20 Opening Remarks

9:20-9:55 Keynote Speech 1
Testing Challenges for Emerging Nanotechnologies
Niraj K. JHA (Princeton University, USA)

9:55-10:30 Keynote Speech 2
Wireless Testing and 3D Integrated Devices: Can They Save Our Jobs?
Cheng-Wen WU (Industrial Technology Research Institute, Taiwan)

10:50-12:00 Plenary Session 2

10:50-11:25 Keynote Speech 3
Can innovations in Test serve as a beacon of light in a dark economy?
Sanjiv TANEJA (Cadence Design Systems, USA)

11:25-12:00 Keynote Speech 4
Challenges and Solutions for Testing TSV-Based 3D-SICs
Erik Jan MARINISSEN (IMEC, Belgium)

13:10-14:30 Session 3A: BIST

CA Based Built-In Self-Test Structure For SoC
Sukanta DAS, Biplab K SIKDAR (Bengal Engineering and Science University, Shibpur - India)

A Random Jitter RMS Estimation Technique for BIST Applications
Jae Wook LEE, Ji Hwan CHUN, Jacob ABRAHAM (The University of Texas at Austin - USA)

A Novel Seed Selection Algorithm for Test Time Reduction in BIST
Rupsa CHAKRABORTY, Dipanwita ROY CHOWDHURY (IIT, Kharagpur - India)

Logic BIST Architecture for System-Level Test and Diagnosis
Jun QIAN (Cisco Systems, Inc. - USA), Xingang WANG, Qinfu YANG, Fei ZHUANG, Junbo JIA, Xiangfeng LI, Yuan ZUO, Jayanth MEKKOTH, Jinsong LIU (SynTest Technologies, Inc. - China), Hao-Jan CHAO (SynTest Technologies, Inc. - Taiwan), Shianling WU, Huafeng YANG, Lizhen YU, FeiFei ZHAO, Laung-Terng WANG (SynTest Technologies, Inc. - USA)

13:10-14:30 Session 3B: Fault Diagnosis

Fault Diagnosis under Transparent-Scan
Irith POMERANZ (Purdue University - USA), Sudhakar REDDY (University of Iowa - USA)

Scan Chain Diagnosis by Adaptive Signal Profiling with Manufacturing ATPG Patterns
Yu HUANG, Wu-Tung CHENG, Ruifeng GUO, Ting-Pu TAI (Mentor Graphics Corporation - USA), Feng-Ming KUO, Yuan-Shih CHEN (Taiwan Semiconductor Manufacturing Company - Taiwan)

On Improving Diagnostic Test Generation for Scan Chain Failures
Xun TANG (University of Iowa - USA), Ruifeng GUO, Wu-Tung CHENG (Mentor Graphics Corporation – USA), Sudhakar REDDY (University of Iowa - USA), Yu HUANG (Mentor Graphics Corporation – USA)

On Scan Chain Diagnosis for Intermittent Faults
Dan ADOLFSSON (NXP Semiconductors - Netherlands), Joanna SIEW (Philips Applied Technologies - Netherlands), Erik Jan MARINISSEN (IMEC - Belgium), Erik LARSSON (Linköpings Universitet - Sweden)

13:10-14:30 Session 3C: Analog and Mixed-signal Testing

Design-for-Test Circuit for the Reduced Code Based Linearity Test Method in Pipelined ADCs with Digital Error Correction Technique
Jin-Fu LIN, Soon-Jyh CHANG (National Cheng-Kung University - Taiwan)

Multi-Tone Testing of Linear and Nonlinear Analog Circuits using Polynomial Coefficients
Suraj SINDIA, Virendra SINGH (Indian Institute of Science - India), Vishwani AGRAWAL (Auburn University - USA)

Low Cost Dynamic Test Methodology for High Precision ΣΔ ADCs
S. KOOK, H. CHOI, V. NATARAJAN, A. CHATTERJEE (Georgia Tech – USA), A. GOMES, S. GOYAL, L. JIN (National Semiconductor Corporation – USA)

Very-Low-Voltage Testing of Amorphous Silicon TFT Circuits
Shiue-Tsung SHEN, Wei-Hsiao LIU, En-Hua MA, James Chien-Mo LI, I-Chun CHENG (National Taiwan University - Taiwan)

14:45-16:05 Session 4A: Industrial Session

Scan Compression Implementation in Industrial Design - Case Study
Dragon HSU (Ralink), Ron PRESS (Mentor Graphics Corp. - USA)

Calibration as a functional test: An ADC case study
Hsiu-Ming (Sherman) CHANG (ITRI), Kuan-Yu LIN, Kwang-Ting (Tim) CHENG

Customized Algorithms for High Performance Memory Test in Advanced Technology Node
Shomo CHEN (Trident), Ning HUANG, Ting-Pu TAI, Actel NIU

A Practical DFT Approach for Complex Low Power Designs
Augusli KIFLI (Faraday), Y.W. CHEN, Y.W. TSAY, K.C. WU

DFT Challenges in Next Generation Multi-media IP
Vishwanath S, Mukund MITTAL (TI), Subrangshu DAS

Yield Ramp up by Scan Chain Diagnosis
Feng-Ming KUO (TSMC), Yuan-Shih CHEN (Taiwan Semiconductor Manufacturing Company - Taiwan)

14:45-16:05 Session 4B: Low-Power Testing

CAT: A Critical-Area-Targeted Test Set Modification Scheme for Reducing Launch Switching Activity in At-Speed Scan Testing
Kazunari ENOKIMOTO, Xiaoqing WEN, Yuta YAMATO, Kohei MIYASE (Kyushu Institute of Technology - Japan), Hiroaki SONE (Fukuoka Industry, Science & Technology Foundation - Japan), Seiji KAJIHARA (Kyushu Institute of Technology - Japan), Masao ASO, Hiroshi FURUKAWA (NEC Micro Systems - Japan)

New Scheme of Reducing Shift and Capture Power Using the X-Filling Methodology
Jiann-Chyi RAU, Tsung-Tang CHEN, Wei-Lin LI, Po-Han WU (Tamkang University - Taiwan)

Deterministic Built-in Self-Test Using Multiple Linear Feedback Shift Registers for Low-Power Scan Testing
Lung-Jen LEE, Wang-Dauh TSENG, Rung-Bin LIN, Chi-Wei YU (Yuan Ze University - Taiwan)

14:45-16:05 Session 4C: On-Line Testing and Silicon Debug

Low Overhead Time-Multiplexed Online Checking: A Case Study of an H.264 Decoder
Ming GAO, Kwang-Ting CHENG (University of California, Santa Barbara - USA)

A FPGA-based Reconfigurable Software Architecture for Highly Dependable Systems
Alberto SCIONTI, Stefano DI CARLO, Paolo PRINETTO (Politecnico di Torino - Italy)

Using Non-Trivial Logic Implications for Trace Buffer-based Silicon Debug
Sandesh PRABHAKAR, Michael HSIAO (Virginia Tech - USA)

A Post-silicon Debug Support Using High-level Design Description
Yeonbok LEE, Tasuku NISHIHARA, Takeshi MATSUMOTO, Masahiro FUJITA (The University of Tokyo - Japan)

16:20-17:40 Session 5A: Delay Testing

A Low Overhead On-chip Path Delay Measurement Circuit
Songwei PEI, Huawei LI, Xiaowei LI (Chinese Academy of Sciences - China)

An Adaptive Test for Parametric Faults Based on Statistical Timing Information
Michihiro SHINTANI, Kazumi HATAYAMA (Semiconductor Technology Academic Research Center - Japan), Takashi SATO (Kyoto University - Japan), Takumi UEZONO (Tokyo Institute of Technology - Japan)

A Delay Measurement Technique Using Signature Registers
Kentaroh KATOH, Toru TANABE, Haque ZAHIDUL, Kazuteru NAMBA, Hideo ITO (Chiba University - Japan)

Functional Built-in Delay Binning and Calibration Mechanism for on-Chip at-Speed Self Test
Chen-I CHUNG, Jyun-Sian JHOU, Ching-Hwa CHENG, Sih-Yan LI (Feng-Chia University - Taiwan)

16:20-17:40 Session 5B: Test Generation (I)

A Practical Approach to Threshold Test Generation for Error Tolerant Circuits
Hideyuki ICHIHARA, Kenta SUTOH, Yuki YOSHIKAWA, Tomoo INOUE (Hiroshima City University - Japan)

Speeding up SAT-based ATPG using Dynamic Clause Activation
Stephan EGGERSGLUESS, Daniel TILLE, Rolf DRECHSLER (University of Bremen - Germany)

N-distinguishing Tests for Enhanced Defect Diagnosis
Gang CHEN, Janusz RAJSKI (University of Iowa - USA), Sudhakar REDDY (University of Iowa - USA), Irith POMERANZ (Purdue University - USA)

Dynamic Compaction in SAT-Based ATPG
Alejandro CZUTRO, Ilia POLIAN, Piet ENGELKE (Albert-Ludwigs-University - Germany), Sudhakar REDDY (University of Iowa - USA), Bernd BECKER (Albert-Ludwigs-University - Germany)

16:20-17:40 Session 5C: System Test

SIRUP: Switch Insertion in RedUndant Pipeline Structures for Yield and Yield/Area Improvement
Mohammad MIRZA-AGHATABAR, Melvin BREUER, Sandeep GUPTA (University of Southern California - USA)

Transaction Level Modeling and Design Space Exploration for SOC Test Architectures
Chin-Yao CHANG, Chih-Yuan HSIAO, Kuen-Jong LEE (National Cheng Kung University - Taiwan), Alan SU (Global Unichip - Taiwan)

Efficient Software-based Self-test Methods for Embedded Digital Signal Processors
Jun-Jie ZHU, Wen-Ching LIN, Jheng-Hao YE, Ming-Der SHIEH (National Cheng Kung University - Taiwan)

Nov. 25, 2009

9:00-10:20 Session 6A: Panel Session (I):
Is Low Power Testing Necessary? What does the Test Industry Truly Need? --> Real Issues and Available Solutions
Organizer/Moderator:
Anis UZZAMAN (Cadence Design Systems, Inc. - USA)

9:00-10:20 Session 6B: DFT

A Scalable Scan Architecture for Godson-3 Multicore Microprocessor
Zichu Qi, Hui LIU, Xiangku LI, Da WANG, Yinhe HAN, Huawei LI, Weiwu HU (Chinese Academy of Sciences - China)

Kiss the Scan Goodbye: A Non-Scan Architecture for High Coverage, Low Test Data Volume and Low Test Application Time
Michael HSIAO, Mainak BANGA (Virginia Tech - USA)

Multiple Scan Trees Synthesis for Test Time/Data and Routing Length Reduction under Output Constraint
Katherine Shu-Min LI, Yu-Chen HUNG, Jr-Yang HUANG (National Sun Yat-Sen University - Taiwan)

Leveraging Partially Enhanced Scan for Improved Observability in Delay Fault Testing
Deepak K.G., Robinson REYNA, Virendra SINGH, Adit SINGH (Indian Institute of Science - India)

9:00-10:20 Session 6C: RF and Analog Testing

BIST Driven Power Conscious Post-Manufacture Tuning of Wireless Transceiver Systems Using Hardware-Iterated Gradient Search
Vishwanath NATARAJAN, Shyam Kumar DEVARAKOND, Shreyas SEN, Abhijit CHATTERJEE (Georgia Institute of Technology - USA)

Self-Calibrating Embedded RF Down-Conversion Mixers
Abhilash GOYAL, Madhavan SWAMINATHAN, Abhijit CHATTERJEE (Georgia Institute of Technology - USA)

A BIST Solution for the Functional Characterization of RF Systems Based on Envelope Response Analysis
Manuel J. BARRAGAN, Rafaella FIORELLI, Diego VAZQUEZ, Adoracion RUEDA, Jose L. HUERTAS (Universidad de Sevilla - Spain)

Exploiting zero-crossing for the analysis of FM modulated analog/RF signals using digital ATE
Nicolas POUS (LIRMM & Verigy - France), Florence AZAIS, Laurent LATORRE, Pascal NOUET (LIRMM - France), Jochen RIVOIR (Verigy - Germany)

10:40-12:00 Session 7A: SoC Test

IEEE 1500 Compatible Interconnect Test with Maximal Test Concurrency
Katherine Shu-Min LI, Yi-Yu LIAO, Yuo-Wen LIU, Jr-Yang HUANG (National Sun Yat-Sen University - Taiwan)

Multiple-Core under Test Architecture for HOY Wireless Testing Platform
Sung-Yu CHEN, Ying-Yen CHEN, Jing-Jia LIOU (National Tsing Hua University - Taiwan)

Partition Based SoC Test Scheduling with Thermal and Power Constraints under Deep Submicron technologies
Chunhua YAO, Kewal K. SALUJA, Parameswaran RAMANATHAN (University of Wisconsin-Madison - USA)

Test Integration for SOC Supporting Very Low-Cost Testers
Chun-Chuan CHI, Chih-Yen LO, Te-Wen KO, Cheng-Wen WU (National Tsing Hua University - Taiwan)

10:40-12:00 Session 7B: Test Generation (II)

Why is Conventional ATPG Not Sufficient for Advanced Low Power Designs?
Krishna CHAKRAVADHANULA, Vivek CHICKERMANE, Brion KELLER, Patrick GALLAGHER, Anis UZZAMAN (Cadence Design Systems - USA)

New Class of Tests for Open Faults with Considering Adjacent Lines
Hiroshi TAKAHASHI, Yoshinobu HIGAMI, Yuzo TAKAMATSU (Ehime University - Japan), Koji YAMAZAKI, Toshiyuki TSUTSUMI (Meiji University - Japan), Hiroyuki YOTSUYANAGI, Masaki HASHIZUME (The University of Tokushima - Japan)

Test Pattern Selection and Customization Targeting Reduced Dynamic and Leakage Power Consumption
Subhadip KUNDU, Krishna Kumar S., Santanu CHATTOPADHYAY (Indian Institute of Technology Kharagpur - India)

Deterministic Algorithms for ATPG under Leakage Constraints
Goerschwin FEY (University of Bremen - Germany)

10:40-12:00 Session 7C: Test Data Compression

Extended Selective Encoding of Scan Slices for Reducing Test Data and Test Power
Jun LIU, Yinhe HAN, Xiaowei LI (Chinese Academy of Sciences - China)

A Multi-Dimensional Pattern Run-Length Method for Test Data Compression
Lung-Jen LEE, Wang-Dauh TSENG, Rung-Bin LIN, Chi-Wei YU

Bit-Operation-Based Seed Augmentation for LFSR Reseeding with High Defect Coverage
Hongxia FANG, Krishnendu CHAKRABARTY (Duke University - USA), Rubin PAREKHJI (Texas Instruments - India)

Nov. 26, 2009

9:00-10:20 Session 8A: Panel Session (II):
Testing Embedded Memories in the Nano-Era: Will the existing approaches survive?
Organizer/Moderator:
Said HAMDIOUI (Delft University of Technology - Netherlands)

9:00-10:20 Session 8B: Fault Modeling & Diagnosis

A Non-intrusive and Accurate Inspection Method for Segment Delay Variabilities
Ying-Yen CHEN, Jing-Jia LIOU (National Tsing Hua University - Taiwan)

Bridging Fault Diagnosis to Identify the Layer of Systematic Defects
Po-Juei CHEN, James Chien-Mo LI (National Taiwan University - Taiwan), Hsing Jasmine CHAO (Taipei Medical University - Taiwan)

Delay Fault Diagnosis in Sequential Circuits
Youssef BENABBOUD, Alberto BOSIO, Luigi DILILLO, Patrick GIRARD, Serge PRAVOSSOUDOVITCH, Arnaud VIRAZEL (LIRMM - France), Olivia RIEWER

A Partially-Exhaustive Gate Transition Fault Model
Brion KELLER, Dale MEEHL, Anis UZZAMAN (Cadence Design Systems - USA), Richard BILLINGS (AMD - USA)

9:00-10:20 Session 8C: Analog and Mixed-signal Testing

An On-Chip Integrator Leakage Characterization Technique and Its Application to Switched Capacitor Circuits Testing
Chen-Yuan YANG, Xuan-Lun HUANG, Jiun Lang HUANG (National Taiwan University - Taiwan)

LFSR-based Performance Characterization of Nonlinear Analog and Mixed-Signal Circuits
Joonsung PARK, Jaeyong CHUNG, Jacob ABRAHAM (The University of Texas at Austin - USA)

A Jitter Characterizing BIST with Pulse-Amplifying Technique
An-Sheng CHAO, Soon-Jyh CHANG (National Cheng Kung University - Taiwan)

A Low-Cost Output Response Analyzer for the Built-in-Self-Test Sigma-Delta Modulator Based on the Controlled Sine Wave Fitting Method
Shao-Feng HUNG, Hao-Chiao HONG, Sheng-Chuan LIANG (National Chiao Tung University - Taiwan)

10:40-12:00 Session 9A: Memory Test

New Developments and Insights in Memory Test Algorithms
A.J. VAN DE GOOR (ComTex - Netherlands), Said HAMDIOUI, Georgi GAYDADJIEV, Zaid AL-ARS (Delft University of Technology - Netherlands)

Testability Exploration of 3-D RAMs and CAMs
Yu-Jen HUANG, Jin-Fu LI (National Central University - Taiwan)

Fault Diagnosis Using Test Primitives in Random Access Memories
Zaid AL-ARS, Said HAMDIOUI (Delft University of Technology - Netherlands)

10:40-12:00 Session 9B: Test Generation (III)

Test Generation for Designs with On-Chip Clock Generators
Xijiang LIN, Mark KASSAB (Mentor Graphics Corp. - USA)

On the Generation of Functional Test Programs for the Cache Replacement Logic
Wilson PEREZ (Universidad del Valle, Universidad Pedagógicay Tecnológica de Colombia - Colombia), Danilo RAVOTTO, Edgar Ernesto Sanchez SANCHEZ, Matteo SONZA REORDA, Alberto TONDA (Politecnico di Torino - Italy)

Compact Test Generation for Small-Delay Defects Using Testable-Path Information
Dong XIANG, Boxue YIN (Tsinghua University - China), Krishnendu CHAKRABARTY (Duke University - USA)

At-Speed Scan Test Method for the Timing Optimization and Calibration
Kun-Han TSAI, Ruifeng GUO, Wu-Tung CHENG (Mentor Graphics Corp. - USA)

10:40-12:00 Session 9C: Defect-Based Testing

M-IVC: Using Multiple Input Vectors to Minimize Aging-induced Delay
Song JIN, Yinhe HAN, Lei ZHANG, Huawei LI, Xiaowei LI, Guihai YAN (Chinese Academy of Sciences - China)

Analysis of Resistive Bridging Defects in a Synchronizer
Hyoung-Kook KIM, Wen Ben JONE (University of Cincinnati - USA), Laung-Terng WANG, Shianling WU (SynTest Technologies - USA)

On-Chip TSV Testing for 3D IC before Bonding Using Sense Amplification
Po-Yuan CHEN, Cheng-Wen WU (National Tsing Hua University - Taiwan), Ding-Ming KWAI (Industrial Technology Research Institute - Taiwan)

Test Pattern Selection for Potentially Harmful Open Defects in Power Distribution Networks
Yubin ZHANG, Lin HUANG, Feng YUAN, Qiang XU (The Chinese University of Hong Kong - Hong Kong)

Keynote Speech

Keynote Speech 1 (Nov. 24th, 9:20-9:55)

Testing Challenges for Emerging Nanotechnologies

Presenter: Niraj K. JHA (Princeton University, USA)

Summary:

The march to miniaturization of semiconductor technology continues. However, Moore's Law does take a toll on Testing Engineers by making manufacturing-time testing ever more difficult. As if the testing challenges posed by the continued CMOS miniaturization were not enough, recognizing that CMOS is approaching its physical limits, new nanotechnologies are emerging with novel logic primitives that pose several new challenges in fault modeling, test generation, fault simulation, and design for testability.

This talk will begin with some of the testing challenges posed by current CMOS technology. Power-aware test has a rich history. However, we will show that temperature-aware test and power-aware test are not necessarily the same. Thus, a similar concerted effort is necessary for developing temperature-aware test techniques. Then we will move on to the test challenges posed by double-gate CMOS technology, such as FinFETs, which are expected to bridge the gap till the 10nm technology node as single-gate CMOS runs out of steam. Temperature-aware test will be even more important for FinFETs. Several nanotechnologies are vying to take us beyond the 10nm technology node, such as resonant tunneling diodes, quantum cellular automata, nanowires, nanotubes, graphene, single electron transistors, quantum computing, etc. We will finally discuss the testing challenges posed by some of these nanotechnologies.

Keynote Speech 2 (Nov. 24th, 9:55-10:30)

Wireless Testing and 3D Integrated Devices: Can They Save Our Jobs?

Presenter: Cheng-Wen WU (Industrial Technology Research Institute, Taiwan)

Summary:

Testing has contributed a significant portion of the cost in manufacturing advanced semiconductor products. To address this issue, we have proposed the HOY test system, which features wireless communication and enhanced embedded test circuits. In this talk, we first provide the concept, architecture, and test flow for future semiconductor products tested by HOY. We then discuss in detail the testing of embedded memories and logic blocks by HOY. A prototype system has been developed and experimental results will be shown. Another thought is about the development cost of a typical system-on-chip (SOC) using state-of-the-art technology---tens of million dollars for a case, and the cost continues to soar with the ever innovating technology. Today, more and more people are thinking about turning to three-dimensional (3D) integration for possible alternatives that provide better or equal performance with lower cost. Stacking dies using the Through-Silicon-Via (TSV) technology has been considered one of the most promising solutions to extending the life of Moore's Law in semiconductor industry, but of course there are problems to be solved before the infrastructure can be set up to support the industry for manufacturing TSV-based 3D integrated devices. In this talk we will also discuss the design and test issues, and possible solutions for 3D integrated devices. A link between HOY and 3D-IC testing will be established as well.

Keynote Speech 3 (Nov. 24th, 10:50-11:25)

Can innovations in Test serve as a beacon of light in a dark economy?

Presenter: Sanjiv Taneja, Cadence Design Systems, USA

Summary:

While it is widely accepted that R&D innovations serve as the growth engine to gain market share and drive

profitability in technology business, tough economic times present some big challenges to that premise. The first challenge is how to innovate when R&D budgets are tight and funding for new breakthrough ideas is limited. The second challenge -- specific to manufacturing test -- is that the true value of Test is cloaked under the myth of "high Cost of Test" leading some semiconductor businesses to stray away from adequate levels of investment that is needed to maintain the quality levels and withstand increasingly fierce competition in the era of economic globalization. Another challenge relates to linking innovation to business strategies when the short-term considerations become a barrier to moving the innovation process forward.

In this talk, we will address some of the solutions to these challenges by drawing upon real life experiences in the area of DFT/ATPG/Diagnostics in a corporate setting. The solutions range from managing innovation with a similar degree of discipline that gets applied to the rest of the business operations, creating an innovation-centric corporate environment, collaborating with customers and universities on high impact problems and creating the sparks of imagination that fuel the innovation process to focusing on rapidly transforming the innovations to complete solutions that meet customers' needs and maximize the return on investment.

Keynote Speech 4 (Nov. 24th, 11:25-12:00)

Challenges and Solutions for Testing TSV-Based 3D-SICs

Presenter: Erik Jan MARINISSEN (IMEC, Belgium)

Summary:

Three-dimensional stacked ICs (3D-SICs) offer dense integration of possibly heterogeneous technologies at a small footprint. Interconnection of the various tiers by means of Through-Silicon Vias (TSVs) promises to increase the interconnect bandwidth and performance while lowering power dissipation and manufacturing cost, and hence might help the semiconductor industry to extend the momentum of Moore's Law into the next decade.

Testing for manufacturing defects is considered by many as a major, still largely unresolved obstacle to make 3D integrated circuits a reality. It is regarded as the "No. 1 Challenge" among all challenges for 3D-SICs (Keynote Speech at the 2007 3D Architecture Conference by Ted Vucurevich, former CTO of Cadence Design Systems). There are concerns about testing cost, and even the feasibility of testing such TSV-based 3D-SICs.

In this presentation, after a review of TSV-based technologies, we present a structured overview of the challenges in testing 3D-SICs, along with solutions as far as available today. Whereas these 'super chips' require most of today's advanced test and DfT approaches, they also have some unique challenges of their own. These include (1) development of new fault models and corresponding tests for thinned-die defects and TSV-based interconnects, (2) wafer probing on small and numerous micro-bumps and/or TSV tips under stringent damage requirements, (3) handling of and probing on wafers with thinned-die stacks, (4) further strengthening of the well-known modular test concept, (5) the design, partitioning, and optimization of DfT architectures that span across multiple dies, and (6) optimization of the test flow for maximum effectiveness and lowest cost.

Tutorials

Tutorial 1

Power-Aware Testing and Test Strategies for Low Power Devices

Presenters:

Patrick Girard (LIRMM/CNRS)
Nicola Nicolici (McMaster University)
Xiaoqing Wen (Kyushu Institute of Technology)

Summary:

Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability.

Tutorial 2

System-in-Package Test Strategies

Presenter:

Yervant Zorian (Virage Logic Corp)

Summary:

Today's miniaturization and performance requirements result in the usage of high density advanced packaging technologies, such as System-in-Package (SiP), 3D integration, Direct Chip Attach, Package-inpackage. Due to their physical access limitation, the complexity and cost associated with their test and diagnosis are considered major issues facing their use. This tutorial provides comprehensive knowledge of test solutions for advanced packages by placing particular emphasis on: test and debug approaches for bare dies; testing schemes for 3D packages, flip-chips used in direct chip attach, and SiP packages; testing bare substrates, and finally test, diagnosis and repair techniques for assembled modules.

Registration

Registration Fees (NT$)

NOTE: At least ONE author of each paper must register at a non-student rate by August 10, 2009

ATS 2009 Registration Fees (The exchange rate is approx. NT$33 to US$1)

Memberships	Until Oct. 10	After Oct. 10
IEEE member	NT$15000	NT$18000
Non-member	NT$19000	NT$22500
IEEE student member	NT$8500	NT$10000
Student non-member	NT$10500	NT$13000

• Student fees do not include the social event (the tour and the banquet).

Registration fees include:
• All sessions
• Proceedings
• Welcome Reception
• Coffee Breaks
• Lunches
• Banquet

ATS 2009 Tutorial Fees (per Tutorial)

Memberships	Until Oct. 10	After Oct. 10
IEEE member	NT$2350	NT$3000
Non-member	NT$3300	NT$4000
IEEE student member	NT$1350	NT$1650
Student non-member	NT$1650	NT$2000

Additional Items (Optional)

Category	Price
Extra pages fees	NT$2700 each X ____ extra page(s) (at most 2)
Extra social event tickets	NT$2000 each X ____ ticket(s)

• Extra pages fee for each paper exceeding page limit must be paid by August 10. Please indicate the paper reference number above.
• After October 10, participating in the social event is not guaranteed.

Please note that:

1. IEEE Member rates are only available to individuals who are IEEE members at the time of registration - visit www.ieee.org to join. IEEE members will be required to show their valid IEEE membership card at the conference registration desk.
2. Student registrants (member or non-member) must provide proof of student status by faxing a copy of his/her university identification (ID) card or a letter from the university signed by an official representative verifying student status. Please fax to: +886-2-8226-2785. Students should be prepared to show their student identification card at the conference registration desk.

Tutorials

Two excellent tutorials are scheduled sequentially on Nov. 23rd. You are encouraged to register for both tutorials.

No.	Time	Topic
1	09:00-12:00	Power-Aware Testing and Test Strategies for Low Power Devices
2	14:00-17:00	System-in-Package Test Strategies

Registration Procedures

You may submit your registration on-line (recommended) or by fax, no later than November 6, 2009. Only on-site registration is possible after this date. Registration by e-mail or by phone will NOT be accepted any time. Please read all the following information carefully before registering.

Registration Methods

1. **On-line Registration**

   On-line registration and payment is recommended. Your registration payment will be processed through either a secure web-based credit card payment system (SSL encrypted data transfer) or bank transfer. Please click here to begin: Online Registration (IE browser suggestion)

2. **Registration by Fax**

   You may also choose to fax the completed registration form (doc, or pdf), containing your credit card or other payment information to: +886-2-8226-2785.
   Local students must register by Fax or Email using student registration form (.doc).

3. **Registration by Mail**(Please kindly arrange the mail to be received by November 15, 2009)

   Registration may also be sent by mail, using the registration form (doc, or pdf). Please mail the completed registration form to

   ATS 2009 Secretariat
   c/o ENJOY PCO
   6F.-9., No.2, Jian 8th Rd., Jhonghe City, Taipei 235
   Tel: +886-2-8226-1010 ext.69 (Mr. Jones Lao)
   Fax:+886-2-8226-2785
   E-mail: ats09@cs.nchu.edu.tw

Payment Methods

All payments must be made in New Taiwan Dollars (NT$). Registration fees can be remitted by credit card (both Visa and MasterCard are acceptable) or bank transfer. Cash payments will only be accepted on site. Credit card payment will also be available on site. Other methods of payment will not be accepted.

1. **On-line credit card payment.** Your credit card statement will show the charge as: ATS2009 Registration Fee. You will also receive the official confirmation of registration via e-mail from the ATS 2009 Secretariat.
2. **Pay by fax.** The ATS 2009 Secretariat will charge your credit card with the respective amount and send you the official confirmation of registration via e-mail.
3. **Pay by bank transfer.** For online registration, please choose the "bank transfer" option in the payment methods to print out the bank transfer form which will include your registration information and the bank wiring information below:

   Bank Name: Bank Of Taiwan
   Bank Address: 23, Linhai 1st Road, Kaohsiung, TAIWAN
   Bank Account Number: 051001089443
   Bank Account Name: Taiwan Institute of Electrical and Electronic Engineering
   Bank Swift Code: BKTWTWTT051

   You should fax both the bank transfer form and bank transfer receipt to +886-6-2381249. Please kindly present this copy at the registration desk. After proof of payment has been confirmed by our bank, you will receive the official confirmation of registration via e-mail from the ATS 2009 Secretariat. Please note that any additional transfer or service charges imposed by the bank must be paid by the participant. Please DO NOT allow your bank to deduct it from the registration fee.

   For registration by fax, the bank transfer information above is already contained in the registration form (doc, or pdf). Please just fax the registration form and bank transfer receipt to +886-2-82262785.

Please note that:

- Your confirmation email will serve as your receipt.
- Each participant must register separately.

- Pre-registration payments must be received by October 10, 2009 for early bird registration. A higher rate will be charged if payment is not RECEIVED by this deadline.
- Please print out the official confirmation of registration e-mail to be presented at the registration desk.

Registration Confirmation

Upon receiving your registration payment, a confirmation letter will be e-mailed to you. Please print out this letter and present it at the registration desk.

Cancellation Policy

Cancellations must be made in writing. This written letter should be sent either by fax (+886-2-8226-2785) or by e-mail (ats09@cs.nchu.edu.tw). The amount of refund depends on the date of cancellation, as follows:

Refund Policy

Before Oct. 10, 2009	After Oct. 10, 2009
100% refund with a deduction of NT$4,200 admin fee	No refund

A refund of all prepaid fees, excluding an administration charge of NT$4,200, will be made if there is a written notification of cancellation submitted by October 10, 2009. No refunds will be made for cancellation received after October 10, 2009.

All refunds will be issued within 30 days after the conference.

On-Site Registration Hours

The ATS 2009 registration desk will be open during the following hours:

Monday	Nov. 23	15:00-17:00
Tuesday	Nov. 24	08:00-17:00
Wednesday	Nov. 25	08:00-17:00
Thursday	Nov. 26	08:00-12:00

Invitation Letter

Participants requiring an invitation letter for visa or for other applications should write to the Conference Secretariat ats09@cs.nchu.edu.tw, specifying the following information:

•The e-mail subject should be “Request for Invitation Letter”
•Name, postal address, and a valid e-mail address.
•IEEE Member number, if applicable.
•Name of session and paper number, if you are presenting a paper.
•Position of the requester as a committee member, speaker, or presenter

Please note that registration payment must be made before requesting an invitation letter. This letter is not an official invitation covering fees and other expenses and does not imply any financial support from the conference.

For more information, please link to the visa page.

Personal Insurance

The organizers cannot be held responsible for accidents to conference participants or accompanying persons, for damage or loss of their personal property, or for cancellation expenses, regardless of cause. Participants should therefore, make their own insurance arrangements. Please consult your local insurance sources regarding coverage.

Hotel Reservations

For further information concerning hotel reservation, please link to the accommodation page.

ACCOMMODATIONS

The Evergreen Laurel Hotel Taichung is offering special rates to attendees of the ATS 09 in Taichung. Please complete this form(or pdf), and return one copy via fax or e-mail by 23, OCT. 2009. (Reservation made after this date would be subject to rooms availability)

ACCOMMODATIONS FEE

Room Type	Room Square	Bed Size (cm)	Fee	Special Rate (Standard Floor)	
			TWD	Single Occupied	Double occupied
Superior Room (US)	29.4 m^2	180*200	$6,400	$ 3,200	$ 3,500
Stnandard Twin Room (ST)	29.4 m^2	110x200*2	$6,400	$ 3,200	$ 3,500

Note : 1) Per room per night 5% government tax & 10% service charge of the original rate are included.
2) A surcharge of TWD 380 will be applied for extra one daily breakfast.
3) Free for internet speedway service.
4) Complimentary fruit basket on the day of arrival.
5) Enjoy unlimited use of the health club, sauna, swimming pool and exercise facilities.

The website of the hotel is http://www.evergreen-hotels.com/branch/content/about/about01.aspx

Alternative Hotels

You can find other hotels in the neighborhood of the venue.
Hotel One
The Splendor Taichung

If you want to stay one of these hotels, please reserve rooms at a hotel on your own.

From Taiwan Taoyuan International Airport (CKS International Airport)

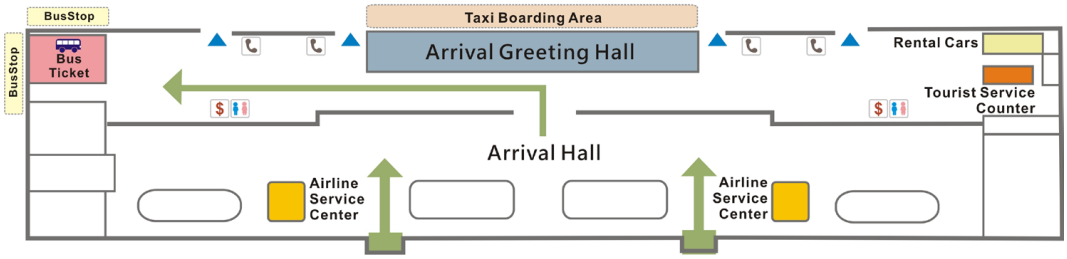
Bus

Bus line: Fe Go Express (飛狗巴士)
Service hours: Taiwan Taoyuan Airport (06:00-01:30) Taichung (02:00-22:00)
Trip duration: 120 mins
Bus Stop: Evergreen Laurel Hotel
Ticket price: Adult NT$270; Child NT$190

Bus line: Taiwan Bus Corp.(Kuokuang Line 國光客運)
Service hours: Taiwan Taoyuan Airport (06:30-22:30) Taichung (05:00-18:20)
Trip duration: 130 mins
Bus Stop: Chung Ming Elementary School
Ticket price: Adult NT$250; Child NT$145

Ticket counters are located in the Arrival Passenger Reception Areas of both Terminals
Terminal I: On the southwest side of the Arrival Passenger Reception Area.
Terminal II: On the northeast side of the Arrival Passenger Reception Area on the first floor of the terminal.

Terminal 1: 1st Floor



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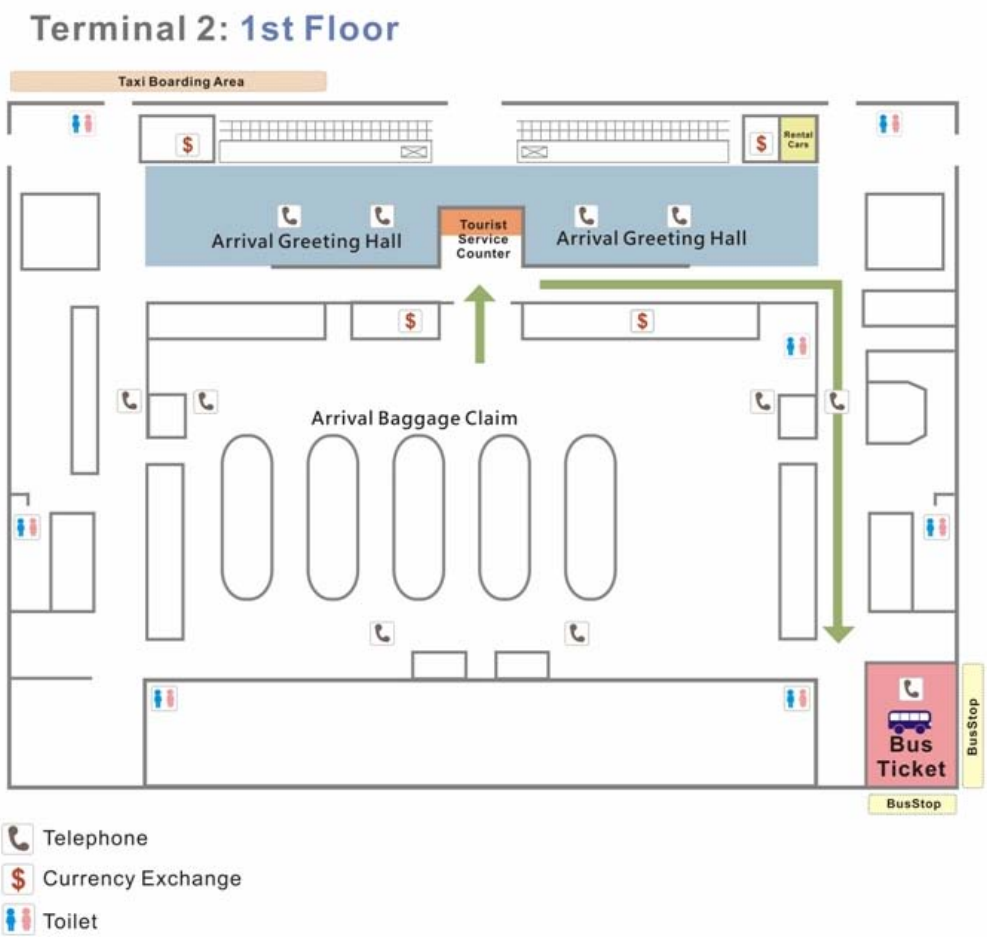

Taiwan High Speed Railway (THSR)

Step1. Shuttle Bus

Bus line: Ubus 705 line
Service hours: Taiwan Taoyuan Airport Terminal 1(06:30-22:30)
THRS Taoyuan Station (07:00-23:45)
Trip duration: 15 mins

Ticket price: Adult NT$30; Child NT$15

Step2. Taiwan High Speed Railway

Service hours: THRS Taoyuan Station (06:52-23:22) THRS Taichung Station (06:30-22:54)
Trip duration: 38 mins
Station: THRS Taichung Station
Ticket price: Stand Class: Adult NT$350; Child NT$270
Business Class: Adult NT$805; Child NT$505
Non-reserved: Adult NT$455; Child NT$250
Timetable: http://www.thsrc.com.tw/download/timetable_090316_en.pdf

Step3. Taxi

Service hours: 06:00-24:00
Trip duration: 20~30 mins
Charge: Typical taxi fare to Evergreen Laurel Hotel is approx. NT$250.

In Taichung City

Driving:

- Get off at the Taichung Chung Kang Rd. interchange from National Rd#1, and drive toward Taichung, and in approximately 2 kilometers you will get off at Evergreen Laurel Hotel (Taichung).

Mass transit:

- Get off at Taichung Railway Station from the Taiwan Railway and then get on routes 27, 106 or 88 of Taichung Passenger Service then get off at Station Hecuo.

- Get off at Taichung Station from the Taiwan High Speed Rail and get on Ubus85 to the intersection of Wenxin Rd. and Chung Kang Rd. then transfer to Ubus83 you will get off at Evergreen Laurel Hotel (Taichung).

Social Program

Nov. 25, 2009, 1:30 pm - 8:00 pm, Sun Moon Lake, Nantou

Tour – Sun Moon Lake

Sun Moon Lake, situated in Nantou County's Yuchih Township, in the center of Taiwan, and is the island's largest lake. It is a beautiful alpine lake, divided by the tiny Lalu Island; the eastern part of the lake is round like the sun and the western side is shaped like a crescent moon, hence the name "Sun Moon Lake". Its crystalline, emerald green waters reflect the hills and mountains which rise on all sides. Natural beauty is enhanced by numerous cultural and historical sites. Well-known both at home and abroad, the Sun Moon Lake Scenic Area has exceptional potential for further growth and recognition as a prime tourism destination. When you visit Sun Moon Lake, we provide 1.5hr travel arrangement by boat. You will have an irresistible impulse to reach the center of the lake, and to come close to the natural beauty of the lakes and mountains.

Banquet – The Lalu

The Lalu is located on Sun Moon Lake's Lalu Peninsula. In the past, the building served as Chiang Kai Shek's travel accommodation. The Lalu's architectural design centres on the themes of utmost simplification of Zen style and is constructed with four major building materials of wood, stone, glass and iron. Its unique "Ongoing Style" of architecture has impressed the public and already becomes a model imitated by restaurants, hotels and various personal and business establishments.

Classical Chinese Music

The Zheng, commonly known as Guzheng, is a plucked string instrument that is part of the zither family. It is one of the most ancient Chinese musi-cal instruments according to the documents written in the Qin dynasty (before 206 BC). Zheng is the forerunner of Japanese koto, Korean kay-agum,

Mongolian yatag, and Vietnamese dan tranh.

Puppet Show

Taiwanese glove puppetry is a drama that is deeply embedded in Taiwanese folk society. In a different era, it served as the Taiwanese people's best outlet for recreation and relaxation. Today, though no longer Taiwan's most important drama activity, glove puppetry continues to adjust to changing trends to offer a glamorous and appealing drama.

Upload

The presentation file upload page is closed.

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Thank you for your contribution to ATS'09.

Visa

Invitation Letter

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·The e-mail subject should be "Request for Invitation Letter"
·Name, postal address, and a valid e-mail address.
·IEEE Member number, if applicable.
·Name of session and paper number, if you are presenting a paper.
·Position of the requester as a committee member, speaker, or presenter

Please note that registration payment must be made before requesting an invitation letter. This letter is not an official invitation covering fees and other expenses and does not imply any financial support from the conference.

Entry without Visa for 30 days is permitted for visitors from the following countries:

Australia、 Austria、 Belgium、 Canada、 Costa Rica、 Czech Republic 、Denmark、Finland、France、Germany、Greece、Ireland、Iceland、Italy、Japan、 Republic of Korea、Liechtenstein、Luxembourg、Malaysia、Malta、Monaco、Netherlands、New Zealand、Norway、Portugal、Singapore、Spain、Sweden、Switzerland、U.K.、U.S.A, etc.

For countries not listed above, further information can be checked at: http://www.boca.gov.tw

Requirements:

1. A passport valid for a least six months
2. A return plane ticket or plane ticket and a visa for the next destination, and a confirmed plane seat.reservation for departure
3. No extension after 30 days

If you are not the countries mentioned above, you need to apply for a Visa.

Visitor Visa for Attending Conference / Exhibition

Requirements		Description
1.	Completed & signed application form	Download (PDF)
2.	Two passport-size photos in color within 6 months	Photo with a white background
3.	Passport (original & photocopy)	Valid for 6 months with blank pages
4.	Evidence of documents	Invitation Letter or proof of exhibition & applicant's ID
5.	Other additional documents may be required during processing	Ticket、 electronic ticket or proof of a travel agency

Procedures：

1. Applicants can lodge their applications with the necessary documents and statutory fee at our .overseas missions
2. Interview may be required when necessary

Requirements:

1. Visas are issued as stipulated by Article 12 of the Statute Governing Issuance of Taiwan Visas for

Foreign Passports. As a sovereign nation, the ROC has the right to refuse applications for visas without providing any explanation for such decisions; visa application fee is not refundable

2. Fee for single entry: US$50 (NT$1,600)；Fee for multiple entry: US$100 (NT$3,200)；Reciprocal processing fee: US$131 (NT$4,323), currently only for American passport holders

Visa for Mainland Chinese Participant

Participants holding a valid PRC passport
中國大陸境內持有中國大陸護照與會者申請入台許可證:

本次大陸人士入台許可證申請委託大會秘書處 樂業國際會議顧問公司辦理
1. 務必於2009年8月31日前完成註冊，並提供註冊編號及以下資料用快遞方式郵寄給大會秘書處，以便協助辦理入台許可証事宜。如未於8月31日寄達相關資料，將會影響來台行程，故請務必確實辦理。

(1)個人基本資料:

中文姓名:
英文姓名:
任職單位:
職 稱:
出生年月日:
Registration ID :
E-Mail:

(2)工作單位在職證明正本: 每人一份，需有單位章及出具日期。(備註：現任職單位，除黨、政、軍職外，另具有「人大代表」、「政協委員」及「台辦」身分者，均應據實填寫)

(3)最高學歷證明影本: 每人一份（例如：教授資格證書，畢業證書或學生證）

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申請來台流程

1. 台灣的申請流程：(約1.5個月)
2009年8月31日前寄達資料給大會秘書處，送交出境管理局進行審核，入台許可証核發後將以快遞寄出

2. 大陸來台人員的申請流程 (僅提供參考：相關申請事宜以貴單位規定為主)★請大家務必抓緊時間辦理★
(1) 務必先向貴學校及單位的國際合作處咨詢來台相關申請流程
(2) 收到入台許可証之前：務必先向貴單位申請來台手續(約1個月)
(3) 收到入台許可証之後：(約2個月)

第一步驟：將台灣的入台許可証批件(通知和複印件、邀請信)向大陸國台辦辦理批件
第二步驟：拿入台許可証批件和國台辦批件到省公安機關辦理出入境手續

3.重要時間點
8月31日:
大陸來台人員完成註冊，並提供註冊編號及申請資料用快遞方式郵寄給大會秘書處

10月15日:
1.大會完成入台許可証之核發並以快遞寄給來台人員。
2.大陸來台人員向貴學校及單位的國際合作處咨詢來台相關申請流程並完成貴單位申請來台手續

11月20日:
大陸來台人員完成大陸國台辦及省公安等相關機關的出入境手續，準備來台

11月22日:
大陸來台人員啟程來台並轉機香港領取來台許可証正本

11月27日:
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Call For Papers

The 18th Asian Test Symposium (ATS' 09)

November 23-26, 2009

Evergreen Laurel Hotel, Taichung, Taiwan

Sponsored by

IEEE Computer Society
Test Technology Technical Council
National Chung Hsing University, Taiwan

In cooperation with

National Tsing Hua University, Taiwan
National Cheng Kung University, Taiwan
National Science Council, Taiwan
Ministry of Education, Taiwan
Industrial Tech. Research Inst., Taiwan
Taiwan Institute of Electrical and Electronics Engineering

Objective

The Asian Test Symposium (ATS) provides an open forum for researchers and engineers from all countries of the world, especially from Asia, to exchange innovative ideas on system, board, and device testing with design, manufacturing and field considerations in mind. The official language of the symposium is English.

Scope

Original contributions on testing are solicited. Topics of interest include, but are not limited to, the following categories:

- Automatic Test Generation / Fault Simulation
- Design for Testability / DfX
- Built-In Self-Test
- Test Data Compression
- Delay Testing
- Design Verification
- Low-power Testing
- Defect-Based Testing / IDDX Testing
- Fault Modeling & Diagnosis
- Memory Test / FPGA Test
- Others
- Analog and Mixed-Signal Test
- RF Testing
- High-Speed I/O Test
- System-on-a-Chip Test
- System-in-Package Test
- Board and System Test
- On-line Testing
- Network Protocol Testing / NoC Testing
- Software Testing
- Economics of Test

Submission

Regular Sessions: The ATS'09 Program Committee invites original, unpublished paper submissions on the above topics. Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. A 50-words abstract and five keywords are also required. All submissions are to be made electronically through the ATS'09 website. Electronic submissions in PDF files are strongly recommended. Detailed instructions for submissions are to be found at the ATS'09 website.

The submission will be considered evidence that upon acceptance the author(s) will prepare the final manuscript (6 pages for regular session) in time for inclusion in the proceedings and will present the paper at the Symposium.

Industrial Sessions: This session will address a wide range of practical problems in IC, board and system test, diagnosis, failure analysis, design verification, and so on.

- The session will consist of short oral presentations.
- A one or two pages of abstract is required for submission.
- Each submission should also include the complete address and designate a contact person and a presenter.
- If accepted, a two-page summary will be included in the final proceedings.

Abstract submissions should be emailed to Industry Chair: Dr. Wu-Tung Cheng (wu-tung_cheng@mentor.com)

Key Dates (Regular Session)

Submission deadline: **May 18, 2009**
Notification of acceptance: **July 10, 2009**
Camera-ready copy: **August 10, 2009**

Key Dates (Industrial Session)

Submission deadline: **June 22, 2009**
Notification of acceptance: **July 10, 2009**
Camera-ready copy: **August 10, 2009**

FURTHER INFORMATION

Email: ats09@cs.nchu.edu.tw

Program at a Glance

Date	Time	Program		
Nov. 23 (Mon.)	09:00-12:00	**Tutorial 1**		
	14:00-17:00	**Tutorial 2**		
	18:30-21:00	**Welcome Reception**		
Nov. 24 (Tue.)	09:00-10:20	**Plenary Session 1**		
	10:20-10:40	***Coffee Break***		
	10:40-12:00	**Plenary Session 2**		
	12:00-13:10	***Lunch***		
	13:10-14:30	**3A:** BIST	**3B:** Fault Diagnosis	**3C:** Analog and Mixed-signal Testing
	14:30-14:45	*Coffee Break*		
	14:45-16:05	**4A:** Industrial Session	**4B:** Low-Power Testing	**4C:** On-Line Testing and Silicon Debug
	16:05-16:20	*Coffee Break*		
	16:20-17:40	**5A:** Delay Testing	**5B:** Test Generation I	**5C:** System Test
Nov. 25 (Wed.)	09:00-10:20	**6A:** Panel Session I	**6B:** DFT	**6C:** RF & Analog Testing
	10:20-10:40	***Coffee Break***		
	10:40-12:00	**7A:** SoC Test	**7B:** Test Generation II	**7C:** Test Data Compression
	11:30-13:30	***Lunch***		
	13:30-18:30	**Social Event**		
	18:30-20:00	***Banquet***		
Nov. 26 (Thu.)	09:00-10:20	**8A:** Panel Session II	**8B:** Fault Modeling & Diagnosis	**8C:** Analog and Mixed-signal Testing
	10:20-10:40	***Coffee Break***		
	10:40-12:00	**9A:** Memory Test	**9B:** Test Generation III	**9C:** Defect-Based Testing

The 18th Asian Test Symposium

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Advance Program

Sponsored by

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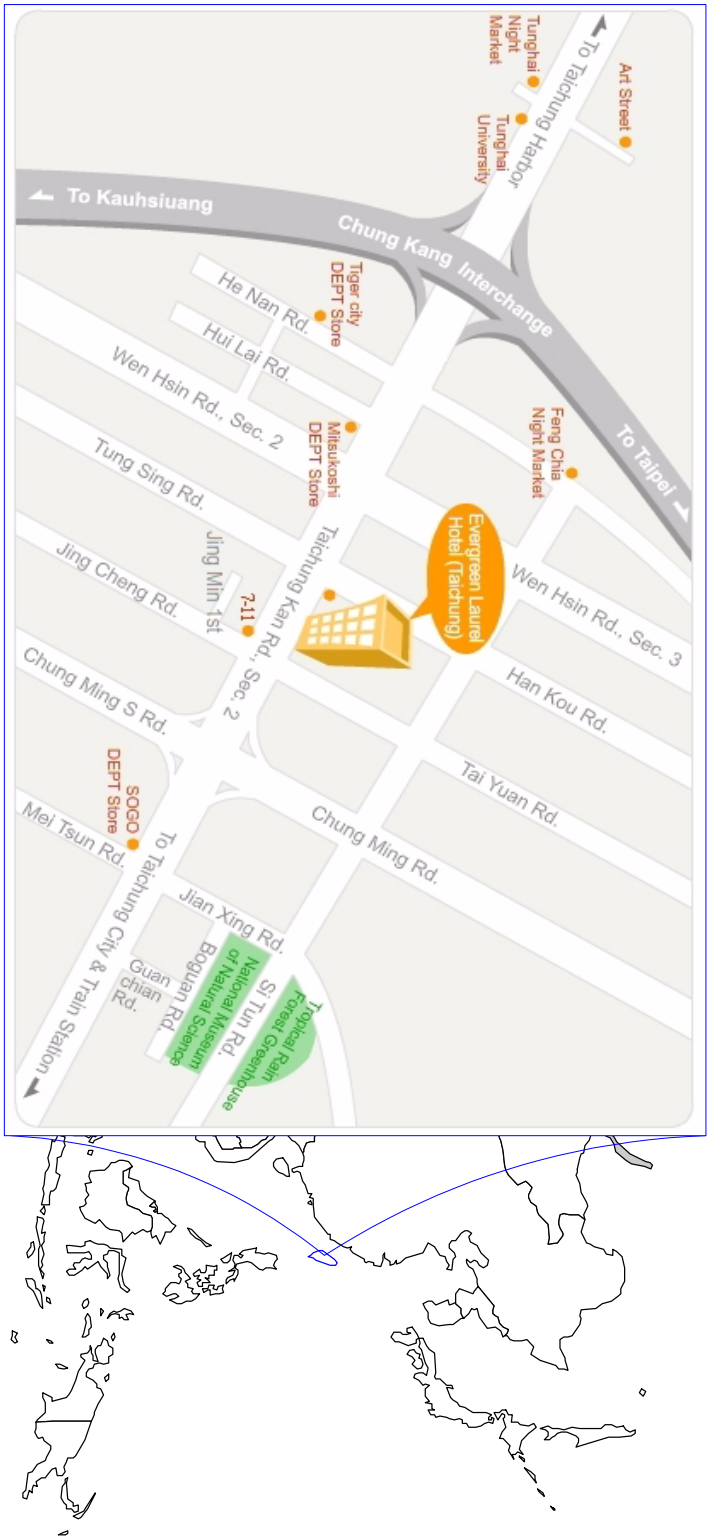

Foreword

Welcome to the Eighteenth Asian Test Symposium (ATS'09). After its debut in Hiroshima, Japan in 1992, the Asian Test Symposium has been held in eighteen cities in Asia and the Pacific Region as the largest symposium that focuses on testing of integrated circuits and systems. Researchers and engineers from all over the world have attended the past symposia and enjoyed discussions. This year the symposium comes to Taichung, Taiwan.

This year, we received 100 technical paper submissions from 16 countries and regions, including 26 from North and South America, 14 from Europe, 26 from Taiwan, seven from Japan, ten from Mainland China, 14 from India, and three from other Asian countries and regions. Each paper was sent to at least three reviewers for evaluation. The program committee meeting was held on July 7, 2009 at the National Chung-Hsing University. Based on the reviewers' rating and comments, 60 regular papers and eight short papers were selected into the final program. The selected papers, which cover nearly all aspects of the key area of VLSI testing, were allocated into 18 technical sessions. We have also selected six industrial papers to form an industry session.

In addition to the technical and industry sessions, the ATS program includes two plenary sessions, two panel sessions and two half-day tutorials. Four keynote addresses in the plenary sessions are given by Professor Niraj K. Jha, Dr. Cheng-Wen Wu, Mr. Sanjiv Taneja and Mr. Erik Jan Marinissen. Two panel sessions are organized by Mr. Anis Uzzaman and Professor Said Hamdioui. Two half-day tutorials are offered in cooperation with the Test Technology Test Education Program (TTEP) of IEEE Computer Society, Test Technology Technical Council (TTTC). One is on low power testing by Dr. Patrick Girard, Dr. Nicola Nicolici, and Dr. Xiaoqing Wen and the other is on system-in-package test by Dr. Yervant Zorian.

Finally we would like to thank the reviewers, the program committee members, the organizing committee members, and the ATS Steering Committee members. We sincerely hope that you will find this event pleasant and enlightening.

Welcome to Taichung and enjoy ATS'09!

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Tutorials

Tutorial I

Power-Aware Testing and Test Strategies for Low Power Devices

9:00 am -12:00 pm, Monday, Nov. 23, Auditorium

Patrick Girard, *LIRMM/CNRS*
Nicola Nicolici, *McMaster University*
Xiaoqing Wen, *Kyushu Institute of Technology*

Summary: Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability.

Tutorial II

System-in-Package Test Strategies

13:30 pm -16:30 pm, Monday, Nov. 23, Auditorium

Yervant Zorian, *Virage Logic Corp*

Summary: Today's miniaturization and performance requirements result in the usage of high density advanced packaging technologies, such as System-in-Package (SiP), 3D integration, Direct Chip Attach, Package-in-package. Due to their physical access limitation, the complexity and cost associated with their test and diagnosis are considered major issues facing their use. This tutorial provides comprehensive knowledge of test solutions for advanced packages by placing particular emphasis on: test and debug approaches for bare dies; testing schemes for 3D packages, flip-chips used in direct chip attach, and SiP packages; testing bare substrates, and finally test, diagnosis and repair techniques for assembled modules.

Plenary Sessions

Opening Remarks

9:00 am - 9:20 am, Tuesday, Nov. 24, Evergreen Ballroom

Shi-Yu Huang, *General Co-chair*
Ming-Der Shieh, *General Co-chair*
Sying-Jyan Wang, *Program Chair*

Keynote Speech I

Testing Challenges for Emerging Nanotechnologies

9:20 am - 9:55 am, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Niraj K. Jha, *Princeton University, USA*

Chair: Chin-Long Wey, *National Chip Implementation Center, Taiwan*

Summary: The march to miniaturization of semiconductor technology continues. However, Moore's Law does take a toll on Testing Engineers by making manufacturing-time testing ever more difficult. As if the testing challenges posed by the continued CMOS miniaturization were not enough, recognizing that CMOS is approaching its physical limits, new nanotechnologies are emerging with novel logic primitives that pose several new challenges in fault modeling, test generation, fault simulation, and design for testability. This talk will begin with some of the testing challenges posed by current CMOS technology. Power-aware test has a rich history. However, we will show that temperature-aware test and power-aware test are not necessarily the same. Thus, a similar concerted effort is necessary for developing temperature-aware test techniques. Then we will move on to the test challenges posed by double-gate CMOS technology, such as FinFETs, which are expected to bridge the gap till the 10nm technology node as single-gate CMOS runs out of steam. Temperature-aware test will be even more important for FinFETs. Several nanotechnologies are vying to take us beyond the 10nm technology node, such as resonant tunneling diodes, quantum cellular automata, nanowires, nanotubes, graphene, single electron transistors, quantum computing, etc. We will finally discuss the testing challenges posed by some of these nanotechnologies.

Keynote Speech II

Wireless Testing and 3D Integrated Devices: Can They Save Our Jobs?

9:55 am - 10:30 am, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Cheng-Wen Wu, *ITRI, Taiwan*

Chair: Kuen-Jong Lee, *National Cheng Kung University, Taiwan*

Summary: Testing has contributed a significant portion of the cost in manufacturing advanced semiconductor products. To address this issue, we have proposed the HOY test system, which features wireless communication and enhanced embedded test circuits. In this talk, we first provide the concept, architecture, and test flow for future semiconductor products tested by HOY. We then discuss in detail the testing of embedded memories and logic blocks by HOY. A prototype system has been developed and experimental results will be shown. Another thought is about the development cost of a typical system-on-chip (SOC) using state-of-the-art technology---tens of million dollars for a case, and the cost continues to soar with the ever innovating technology. Today, more and more people are thinking about turning to three-dimensional (3D) integration for possible alternatives that provide better or equal performance with lower cost. Stacking dies using the Through-Silicon-Via (TSV) technology has been considered one of the most promising solutions to extending the life of Moore's Law in semiconductor industry, but of course there are problems to be solved before the infrastructure can be set up to support the industry for manufacturing TSV-based 3D integrated devices. In this talk we will also discuss the design and test issues, and possible solutions for 3D integrated devices. A link between HOY and 3D-IC testing will be established as well.

Keynote Speech III

Can Innovations in Test Serve as a Beacon of Light in a Dark Economy?

10:50 am -11:25 am, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Sanjiv Taneja, *Cadence Design Systems, USA*

Chair: Shi-Yu Huang, *National Tsing Hua University Taiwan*

Summary: While it is widely accepted that R&D innovations serve as the growth engine to gain market share and drive profitability in technology business, tough economic times present some big challenges to that premise. The first challenge is how to innovate when R&D budgets are tight and funding for new breakthrough ideas is limited. The second challenge -- specific to manufacturing test -- is that the true value of Test is cloaked under the myth of "high Cost of Test" leading some semiconductor businesses to stray away from adequate levels of investment that is needed to maintain the quality levels and withstand increasingly fierce competition in the era of economic globalization. Another challenge relates to linking innovation to business strategies when the short-term considerations become a barrier to moving the innovation process forward.

In this talk, we will address some of the solutions to these challenges by drawing upon real life experiences in the area of DFT/ATPG/Diagnostics in a corporate setting. The solutions range from managing innovation with a similar degree of discipline that gets applied to the rest of the business operations, creating an innovation-centric corporate environment, collaborating with customers and universities on high impact problems and creating the sparks of imagination that fuel the innovation process to focusing on rapidly transforming the innovations to complete solutions that meet customers' needs and maximize the return on investment.

Keynote Speech IV

Challenges and Solutions for Testing TSV-Based 3D-SICs

11:25 am -12:00 pm, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Erik Jan Marinissen, *IMEC, Belgium*

Chair: Ming-Der Shieh, *National Cheng Kung University, Taiwan*

Summary: Three-dimensional stacked ICs (3D-SICs) offer dense integration of possibly heterogeneous technologies at a small footprint. Interconnection of the various tiers by means of Through-Silicon Vias (TSVs) promises to increase the interconnect bandwidth and performance while lowering power dissipation and manufacturing cost, and hence might help the semiconductor industry to extend the momentum of Moore's Law into the next decade. Testing for manufacturing defects is considered by many as a major, still largely unresolved obstacle to make 3D integrated circuits a reality. It is regarded as the "No. 1 Challenge" among all challenges for 3D-SICs (Keynote Speech at the 2007 3D Architecture Conference by Ted Vucurevich, former CTO of Cadence Design Systems). There are concerns about testing cost, and even the feasibility of testing such TSV-based 3D-SICs. In this presentation, after a review of TSV-based technologies, we present a structured overview of the challenges in testing 3D-SICs, along with solutions as far as available today. Whereas these 'super chips' require most of today's advanced test and DfT approaches, they also have some unique challenges of their own. These include (1) development of new fault models and corresponding tests for thinned-die defects and TSV-based interconnects, (2) wafer probing on small and numerous micro-bumps and/or TSV tips under stringent damage requirements, (3) handling of and probing on wafers with thinned-die stacks, (4) further strengthening of the well-known modular test concept, (5) the design, partitioning, and optimization of DfT architectures that span across multiple dies, and (6) optimization of the test flow for maximum effectiveness and lowest cost.

Panel Discussions

Panel Session I

Is Low Power Testing Necessary? What does the Test Industry Truly Need?
Real Issues and Available Solutions

9:00 am -10:20 am, Wednesday, Nov. 25, Laurel Salon I

Organizer/Moderator: Anis Uzzaman – *Cadence Design Systems, Inc., USA*

Potential Panelists: Xiaoqing Wen –*Kyushu Institute of Technology, Japan*
Kazumi Hatayama – *STARC, Japan*
Sanjiv Taneja – *Cadence Design Systems, Inc., USA*
Erik Jan Marinissen – *IMEC, Belgium*

Abstract: With the changing face of the consumer driven semiconductor industry, there are new challenges facing the industry which need to be resolved. Minimizing Power dissipation is a significant and growing challenge with the growth of the wireless and portable device segments and with the need to be 'green'. Even during manufacturing test, power is definitely among the top ten items needing attention and expertise. Since 90-nm there has been a recognition that power consumption during test can be a factor affecting product quality and yield. Excessive power consumption during manufacturing test affects the reliability of digital integrated circuits, leading to power-driven failures and higher infant mortality. These trends if continuing on their present course will force designers to adopt specific power management and low power design techniques for manufacturing test.

Power consumption during functional operation is no longer the only area of concern. Power is increasingly becoming an issue during various manufacturing test modes of the circuit operation. It has been found in several studies that the normal scan test mode power consumption is several times higher than the functional power consumption in existing designs. While typical test mode power consumption limits are usually around 2X functional power, field testing requires test power to be as low as worst-case functional power. Also, burn-in test and high-voltage testing of chips becomes more difficult as power consumption increases significantly with elevated voltages and temperatures.

There are several reasons why test power is higher than functional power. One of the reasons is that during the test phase simultaneous testing of multiple modules is done to reduce test costs in general. This might not necessarily be true during functional operation. Redundant switching in circuit logic during scan shift and unduly high switching during scan shift/capture also adds up to the high power consumption of the circuit during test. Higher frequency operation of scan chains during Built-in-self-test (BIST) can also result in more power consumption during test comparing to circuit's functional operation. With at-speed transition fault patterns becoming a necessary component of all test suites supplied to production engineers, fast at-speed capture pulses in scan transition pattern tests can cause undue peak power spikes or IR drop issues. Also, increasing frequency of scan shift as tester supplied clock frequency increases might

be another reason why test operation can consume more power than the functional operation of the circuit.

In an ideal profile for developing and implementing a manufacturing test power reduction strategy, the power reduction effectiveness is expected to be high and usable with on-chip compression. The test coverage impact is also expected to be low and there must be minimum impact on ATPG tools and flows. On the other side, the test data volume and test time should not be impacted by the power reduction strategy. Finally, the strategy must not impact physical design care-abouts and functional timing. Obviously, the power reduction strategy is complex but must not place production at risk.

Various power reduction and power management techniques have been proposed in the literature some of which are deployed in chips manufactured today using commercial low-power design tools. Two such examples of power management techniques are clock gating and power domain partitioning. DFT Insertion is another technique for reducing test power. The combinational circuit toggling that happens during scan shift can be eliminated (reduced) if blocking circuitry can be incorporated at all (some) Q outputs of the scan flip flops. Scan segmentation/partitioning is another DFT technique using which power during test can be controlled.

Low-power scan partitioning has been shown to be feasible on commercial designs such as the CELL processor. Some of the other DFT techniques for reducing test power include data gating, wherein, for a design with modules A and B, test points are added that allow for scan in of zeros into the scan chains of module A, while module B is tested, and vice versa. Staggered Clocking is another method using which test power consumption is controlled today during test in many designs.

Aside from the above mentioned DFT based power reduction techniques, some of the ATPG techniques are also used for reduced power consumption; intelligent care bit filling has been known as one of the effective methods to gain considerable reduction in power consumption. Various X-fill techniques have been proposed in the literature including 0-fill, adjacent fill, repeat fill, preferred fill, and so on. Another item that should also be given serious thought is the testing of the power management circuitry – power controller, power switches, retention flops, etc. – that is inserted for the functional power control. In many cases, the power management components themselves are overlooked during manufacturing test, there are many questions as how to test the new power management/reduction structures, how to handle these structures while testing the rest of the chip and how to leverage these structures when testing multiple power domains.

With so many open options available for power reduction during test, it is still very difficult to identify the right technique to use for a certain technology device. Also, it is still difficult to identify any power related issue during testing as it is typically identified through prediction and analysis at the ATE. In addition, with all the low power standardization going on in the test industry, it is very confusing for a designer on which standard to follow and adopt.

Some of the major questions that can be the focus of discussion during this panel session are:

- How much of low power issues the test industry is experiencing today?
- Is "POWER DURING TEST" really an issue or just a rumor? If this is a reality then for what process technology we are seeing this to be an issue?
- Is there any easy way to isolate the low power issue occurring during test? What are the specific symptoms?
- What are the measures that people take in general for handling the low power issues today?
- What are the future "TO DOs" in the area of lower geometry technologies.

The objective of this panel is to provide a comprehensive understanding of the power problem during test, outline the various challenges involved, and discuss various existing and emerging solutions to tackle them.

Panel Session II

Testing Embedded Memories in the Nano-Era: Will the existing approaches survive?

9:00 am -10:20 am, Thursday, Nov. 26, Laurel Salon I

Organizer/Moderator: Said Hamdioui, *Delft Univ. of Technology, Netherlands*

Panelists: Jin-Fu Li – National Central University, Taiwan
Ting-Pu Tai – Mentor Graphics, USA
Ad. J. van de Goor – ComTex/TUDelft, the Netherlands
Cheng-Wen Wu – National Tsing Hua University, Taiwan
Shianling Wu – SynTest Technologies, USA

Summary:

Embedded memories have become the fastest growing segment of Systems on Chip (SoC) in recent years. According to the International Technology Roadmap for Semiconductors, embedded memories will continue to dominate the increasing SoC chip area in the future, approaching 94% within one decade. Hence, these memories will severely impact all aspects of SoC manufacturing including yield, quality and reliability. Additionally, nano-technology is causing higher levels of device-parameter variations and new failure mechanisms that are not yet fully understood. Consequently, the existing fault models and test approaches may be not adequate to test embedded memories in the nano-era. Therefore, a radical paradigm change may be needed.

The panel aims at gathering opinions on the different ways to deal with test challenges of embedded memories in the nano-era. The main question is how to deal with this shift in failure mechanisms in order to keep an acceptable product quality at affordable cost. Can the existing test approaches do the job? Do we need to rely more on stresses rather than the algorithms themselves? However, too much stress/ Burn-in may degrade the lifetime of the chip. Do we need to move more towards DFT rather than March tests? Is programmable DFT the ideal solution? Can on-the-fly detect/repair and reconfigure be the answer? Or do we need completely new approaches?

On-Site Registration

Payment: Only credit card or cash will be accepted.

Place: Hallway in Level B2, Evergreen Laurel Hotel, Taichung

Time: Tutorials 09:00 am - 05:00 pm, Nov. 23

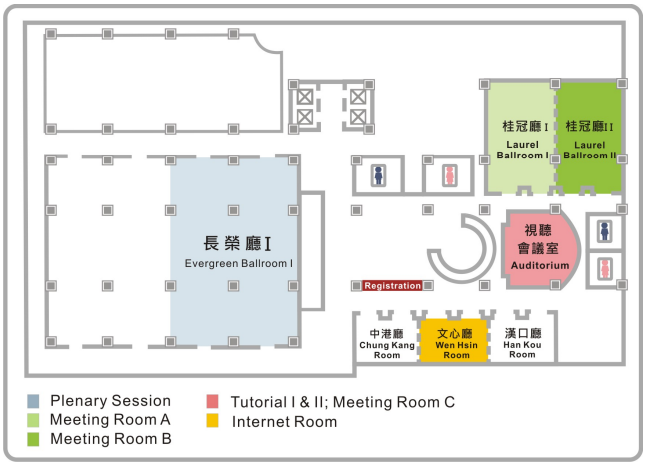
Symposium 08:00 am - 05:00 pm, Nov. 24
08:00 am -12:00 pm, Nov. 25
08:00 am -12:00 pm, Nov. 26

Hotel Information

The Evergreen Laurel Hotel Taichung is offering special rates to attendees of the ATS 09 in Taichung. The number of budget rooms is limited and is on a first-come-first-serve basis. The reservation form can be downloaded from http://ats09.nchu.edu.tw.

Site Map

Level B2, Evergreen Laurel Hotel, Taichung



Technical Paper Sessions

Session 3A: Built-In Self-Test

Time: 13:10 pm - 14:30 pm, Tuesday, Nov. 24, 2009
Place: Laurel Salon I
Chair: *Yinhe Han, Chinese Academy of Sciences, China*

3A-1 CA Based Built-In Self-Test Structure for SoC
Sukanta Das and Biplab K. Sikdar

3A-2 A Random Jitter RMS Estimation Technique for BIST Applications
Jae Wook Lee, Ji Hwan Chun, and Jacob A. Abraham

3A-3 A Novel Seed Selection Algorithm for Test Time Reduction in BIST
Rupsa Chakraborty and Dipanwita Roy Chowdhury

3A-4 Logic BIST Architecture for System-Level Test and Diagnosis
Jun Qian, Xingang Wang, Qinfu Yang, Fei Zhuang, Junbo Jia, Xiangfeng Li, Yuan Zuo, Jayanth Mekkoth, Jinsong Liu, Hao-Jan Chao, Shianling Wu, Huafeng Yang,Lizhen Yu, FeiFei Zhao, and Laung-Terng Wang

Session 3B: Fault Diagnosis

Time: 13:10 pm - 14:30 pm, Tuesday, Nov. 24, 2009
Place: Laurel Salon II
Chair: *Xiaoqing Wen, Kyushu Institute of Technology, Japan*

3B-1 Fault Diagnosis under Transparent-Scan
Irith Pomeranz and Sudhakar M. Reddy

3B-2 Scan Chain Diagnosis by Adaptive Signal Profiling with Manufacturing ATPG Patterns
Yu Huang, Wu-Tung Cheng, Ruifeng Guo, Ting-Pu Tai, Feng-Ming Kuo, and Yuan-Shih Chen

3B-3 On Improving Diagnostic Test Generation for Scan Chain Failures
Xun Tang, Ruifeng Guo, Wu-Tung Cheng, Sudhakar M. Reddy, and Yu Huang

3B-4 On Scan Chain Diagnosis for Intermittent Faults
Dan Adolfsson, Joanna Siew, Erik Jan Marinissen, and Erik Larsson

Session 3C: Analog and Mixed-Signal Testing I

Time: 13:10 pm - 14:30 pm, Tuesday, Nov. 24, 2009

Place: Auditorium

Chair: *Hao-Chiao Hong, National Chiao Tung University, Taiwan*

3C-1 Design-for-Test Circuit for the Reduced Code Based Linearity Test Method in Pipelined ADCs with Digital Error Correction Technique
Jin-Fu Lin, Soon-Jyh Chang, and Chih-Hao Huang

3C-2 Multi-tone Testing of Linear and Nonlinear Analog Circuits Using Polynomial Coefficients
Suraj Sindia, Virendra Singh, and Vishwani D. Agrawal

3C-3 Low Cost Dynamic Test Methodology for High Precision ΔΔ ADCs
S. Kook, Hyun Choi, Vishwanath Natarajan, Abhijit Chatterjee, Alfred Gomes, Shalahb Goyal, and Le Jin

3C-4 Very-Low-Voltage Testing of Amorphous Silicon TFT Circuits
Shiue-Tsung Shen, Wei-Hsiao Liu, En-Hua Ma, James Chien-Mo Li, and I-Chun Cheng

Session 4A: Industrial Session

Time: 14:45 pm - 16:05 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon I

Chair: *Wu-Tung Cheng, Mentor Graphics Corporation, USA*

4A-1 Scan Compression Implementation in Industrial Design - Case Study
Dragon Hsu and Ron Press

4A-2 Calibration as a Functional Test: An ADC Case Study
Hsiu-Ming Chang, Kuan-Yu Lin, and Kwang-Ting Cheng

4A-3 Customized Algorithms for High Performance Memory Test in Advanced Technology Node
Shomo Chen, Ning Huang, Ting-Pu Tai, and Actel Niu

4A-4 A Practical DFT Approach for Complex Low Power Designs
Augusli Kifli, Y.W. Chen, Y.W. Tsay, and K.C. Wu

4A-5 DFT Challenges in Next Generation Multi-media IP
Mukund Mittal, Subrangshu Das, and S. Vishwanath

4A-6 Yield Ramp up by Scan Chain Diagnosis
Feng-Ming Kuo and Yuan-Shih Chhen

Session 4B: Low-Power Testing

Time: 14:45 pm - 16:05 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon II

Chair: *Patrick Girard, LIRMM, France*

4B-1 CAT: A Critical-Area-Targeted Test Set Modification Scheme for Reducing Launch Switching Activity in At-Speed Scan Testing
K. Enokimoto, X. Wen, Y. Yamato, K. Miyase, H. Sone, S. Kajihara, M. Aso, and H. Furukawa

4B-2 New Scheme of Reducing Shift and Capture Power Using the X-Filling Methodology
Tsung-Tang Chen, Wei-Lin Li, Po-Han Wu, and Jiann-Chyi Rau

4B-3 Deterministic Built-In Self-Test Using Multiple Linear Feedback Shift Registers for Low-Power Scan Testing
Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chi-Wei Yu

Session 4C: On-Line Testing and Silicon Debug

Time: 14:45 pm - 16:05 pm, Tuesday, Nov. 24, 2009

Place: Auditorium

Chair: *Chih-Tsun Huang, National Tsing Hua University, Taiwan*

4C-1 Low Overhead Time-Multiplexed Online Checking: A Case Study of An H.264 Decoder
Ming Gao and Kwang-Ting Cheng

4C-2 A FPGA-Based Reconfigurable Software Architecture for Highly Dependable Systems
Stefano Di Carlo, Paolo Prinetto, and Alberto Scionti

4C-3 Using Non-trivial Logic Implications for Trace Buffer-Based Silicon Debug
Sandesh Prabhakar and Michael Hsiao

4C-4 A Post-Silicon Debug Support Using High-Level Design Description
Yeonbok Lee, Tasuku Nishihara, Takeshi Matsumoto, and Masahiro Fujita

Session 5A: Delay Testing

Time: 16:20 pm - 17:40 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon I

Chair: *Jing-Jia Liou, National Tsing Hua University, Taiwan*

5A-1 A Low Overhead On-Chip Path Delay Measurement Circuit
Songwei Pei, Huawei LI, and Xiaowei LI

5A-2 An Adaptive Test for Parametric Faults Based on Statistical Timing Information
Michihiro Shintani, Takumi Uezono, Tomoyuki Takahashi, Hiroyuki Ueyama, Takashi Sato, Kazumi Hatayama, Takashi Aikyo, and Kazuya Masu

5A-3 A Delay Measurement Technique Using Signature Registers
Kentaroh Katoh, Toru Tanabe, Haque Md Zahidul, Kazuteru Namba, and Hideo Ito

5A-4 Functional Built-In Delay Binning and Calibration Mechanism for On-Chip at-Speed Self Test
Chen-I Chung, Jyun-Sian Jhou, Ching-Hwa Cheng, and Sih-Yan Li

Session 5B: Test Generation I

Time: 16:20 pm - 17:40 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon II

Chair: *James Chien-Mo Li, National Taiwan University, Taiwan*

5B-1 A Practical Approach to Threshold Test Generation for Error Tolerant Circuits
Hideyuki Ichihara, Kenta Sutoh, Yuki Yoshikawa, and Tomoo Inoue

5B-2 Speeding up SAT-Based ATPG Using Dynamic Clause Activation
Stephan Eggersglüß, Daniel Tille, and Rolf Drechsler

5B-3 N-distinguishing Tests for Enhanced Defect Diagnosis
Gang Chen, Janusz Rajski, Sudhakar Reddy, and Irith Pomeranz

5B-4 Dynamic Compaction in SAT-Based ATPG
Alexander Czutro, Ilia Polian, Piet Engelke, Sudhakar M. Reddy, and Bernd Becker

Session 5C: System Test

Time: 16:20 pm - 17:40 pm, Tuesday, Nov. 24, 2009

Place: Auditorium

Chair: *Yu Huang, Mentor Graphics Corporation, USA*

5B-5 SIRUP: Switch Insertion in RedUndant Pipeline Structures for Yield and Yield/Area Improvement
Mohammad Mirza-Aghatabar, Melvin A. Breuer, and Sandeep K. Gupta

5B-6 Transaction Level Modeling and Design Space Exploration for SOC Test Architectures
Chin-Yao Chang, Chih-Yuan Hsiao, Kuen-Jong Lee, and Alan P. Su

5B-7 Efficient Software-Based Self-Test Methods for Embedded Digital Signal Processors
Jun-Jie Zhu, Wen-Ching Lin, Jheng-Hao Ye, and Ming-Der Shieh

Session 6A: Panel Session I

Time: 9:00 am - 10:20 am, Wednesday, Nov. 25, 2009

Place: Laurel Salon I

Moderator: *Anis Uzzaman, Cadence Design Systems, Inc., USA*

6A-1 Is Low Power Testing Necessary? What does the Test Industry Truly Need?

Session 6B: DFT

Time: 9:00 am - 10:20 am, Wednesday, Nov. 25, 2009

Place: Laurel Salon II

Chair: *Dong Xiang, Tsinghua University, China*

6B-1 A Scalable Scan Architecture for Godson-3 Multicore Microprocessor
Zichu Qi, Hui Liu, Xiangku Li, Da Wang, Yinhe Han, Huawei Li, and Weiwu Hu

6B-2 Kiss the Scan Goodbye: A Non-scan Architecture for High Coverage, Low Test Data Volume and Low Test Application Time
Michael S. Hsiao and Mainak Banga

6B-3 Multiple Scan Trees Synthesis for Test Time/Data and Routing Length Reduction under Output Constraint
Katherine Shu-Min Li, Yu-Chen Hung, and Jr-Yang Huang

6B-4 Leveraging Partially Enhanced Scan for Improved Observability in Delay Fault Testing
Deepak K.G., Robinson Reyna, Virendra Singh, and Adit D. Singh

Session 6C: RF and Analog Testing

Time: 9:00 am - 10:20 am, Wednesday, Nov. 25, 2009

Place: Auditorium

Chair: *Jiun-Lang Huang, National Taiwan University, Taiwan*

6C-1 BIST Driven Power Conscious Post-Manufacture Tuning of Wireless Transceiver Systems Using Hardware-Iterated Gradient Search
Vishwanath Natarajan, Shyam Kumar Devarakond, Shreyas Sen, and Abhijit Chatterjee

6C-2 Self-Calibrating Embedded RF Down-Conversion Mixers
Abhilash Goyal, Madhavan Swaminathan, and Abhijit Chatterjee

6C-3 A BIST Solution for the Functional Characterization of RF Systems Based on Envelope Response Analysis
Manuel J. Barragán, Rafaella Fiorelli, Diego Vázquez, Adoración Rueda, and José L. Huertas

6C-4 Exploiting Zero-Crossing for the Analysis of FM Modulated Analog/RF Signals Using Digital ATE
Nicolas Pous, Florence Azaïs, Laurent Latorre, Pascal Nouet, and Jochen Rivoir

Session 7A: SoC Test

Time: 10:40 am - 12:00 pm, Wednesday, Nov. 25, 2009

Place: Laurel Salon I

Chair: *Erik Jan Marinissen , IMEC, Belgium*

7A-1 IEEE 1500 Compatible Interconnect Test with Maximal Test Concurrency
Katherine Shu-Min Li, Yi-Yu Liao, Yuo-Wen Liu, and Jr-Yang Huang

7A-2 Multiple-Core under Test Architecture for HOY Wireless Testing Platform
ung-Yu Chen, Ying-Yen Chen, Chun-Yu Yang, and Jing-Jia Liou

7A-3 Partition Based SoC Test Scheduling with Thermal and Power Constraints under Deep Submicron Technologies
Chunhua Yao, Kewal K. Saluja, and Parameswaran Ramanathan

7A-4 Test Integration for SOC Supporting Very Low-Cost Testers
Chun-Chuan Chi, Chih-Yen Lo, Te-Wen Ko, and Cheng-Wen Wu

Session 7B: Test Generation II

Time: 10:40 am - 12:00 pm, Wednesday, Nov. 25, 2009

Place: Laurel Salon II

Chair: *Michael Hsiao, Virginia Tech, USA*

7B-1 Why is Conventional ATPG Not Sufficient for Advanced Low Power Designs?
Krishna Chakravadhanula, Vivek Chickermane, Brion Keller, Patrick Gallagher, and Anis Uzzaman

7B-2 New Class of Tests for Open Faults with Considering Adjacent Lines
Hiroshi Takahashi, Yoshinobu Higami, Yuzo Takamatsu, Koji Yamazaki, Toshiyuki Tsutsumi, Hiroyuki Yotsuyanagi, and Masaki Hashizume

7B-3 Test Pattern Selection and Customization Targeting Reduced Dynamic and Leakage Power Consumption
Subhadip Kundu, Krishna Kumar S., and Santanu Chattopadhyay

7B-4 Deterministic Algorithms for ATPG under Leakage Constraints
Görschwin Fey

Session 7C: Test Data Compression

Time: 10:40 am - 12:00 pm, Wednesday, Nov. 25, 2009

Place: Auditorium

Chair: *Kazumi Hatayama, STARC, Japan*

7C-1 Extended Selective Encoding of Scan Slices for Reducing Test Data and Test Power
Jun Liu, Yinhe Han, and Xiaowei Li

7C-2 A Multi-dimensional Pattern Run-Length Method for Test Data Compression
Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chen-Lun Lee

7C-3 Bit-Operation-Based Seed Augmentation for LFSR Reseeding with High Defect Coverage
Hongxia Fang, Krishnendu Chakrabarty, and Rubin Parekhji

Session 8A: Panel Session II

Time: 9:00 am - 10:20 am, Thursday, Nov. 26, 2009

Place: Laurel Salon I

Chair: *Said Hamdioui, Delft Univ. of Technology, Netherlands*

8A-1 Testing Embedded Memories in the Nano-Era: Will the Existing Approaches Survive?
Said Hamdioui

Session 8B: Fault Modeling & Diagnosis

Time: 9:00 am - 10:20 am, Thursday, Nov. 26, 2009

Place: Laurel Salon II

Chair: *Michel Renovell, LIRMM, France*

8B-1 A Non-Intrusive and Accurate Inspection Method for Segment Delay Variabilities
Ying-Yen Chen and Jing-Jia Liou

8B-2 Bridging Fault Diagnosis to Identify the Layer of Systematic Defects
Po-Juei Chen, James Chien-Mo Li, and Hsing Jasmine Chao

8B-3 Delay Fault Diagnosis in Sequential Circuits
Youssef Benabboud, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, and Olivia Riewer

8B-4 A Partially-Exhaustive Gate Transition Fault Model
Brion Keller, Dale Meehl, Anis Uzzaman, and Richard Billings

Session 8C: Analog and Mixed-Signal Testing II

Time: 9:00 am - 10:20 am, Thursday, Nov. 26, 2009

Place: Auditorium

Chair: *Soon-Jyh Chang, National Cheng Kung University, Taiwan*

8C-1 An On-Chip Integrator Leakage Characterization Technique and Its Application to Switched Capacitor Circuits Testing
Chen-Yuan Yang, Xuan-Lun Huang, and Jiun-Lang Huang

8C-2 LFSR-Based Performance Characterization of Nonlinear Analog and Mixed-Signal Circuits
Joonsung Park, Jaeyong Chung, and Jacob A. Abraham

8C-3 A Jitter Characterizing BIST with Pulse-Amplifying Technique
An-Sheng Chao and Soon-Jyh Chang

8C-4 A Low-Cost Output Response Analyzer for the Built-in-Self-Test .-Δ Modulator Based on the Controlled Sine Wave Fitting Method
Shao-Feng Hung, Hao-Chiao Hong, and Sheng-Chuan Liang

Session 9A: Memory Test

Time: 10:40 am - 12:00 pm, Thursday, Nov. 26, 2009

Place: Laurel Salon I

Chair: *Shyue-Kung Lu, National Taiwan University of Science and Technology, Taiwan*

9A-1 New Algorithms for Address Decoder Delay Faults and Bit Line Imbalance Faults
Ad J. van de Goor, Said Hamdioui, Georgi N. Gaydadjiev, and Zaid Al-Ars

9A-2 Testability Exploration of 3-D RAMs and CAMs
Yu-Jen Huang and Jin-Fu Li

9A-3 Fault Diagnosis Using Test Primitives in Random Access Memories
Zaid Al-Ars and Said Hamdioui

Session 9B: Test Generation III

Time: 10:40 pm - 12:00 pm, Thursday, Nov. 26, 2009

Place: Laurel Salon II

Chair: *Hiroshi Takahashi, Ehime University, Japan*

9B-1 Test Generation for Designs with On-Chip Clock Generators
Xijiang Lin and Mark Kassab

9B-2 On the Generation of Functional Test Programs for the Cache Replacement Logic
W. Perez, D. Ravotto, E. Sanchez, M. Sonza Reorda, and A. Tonda

9B-3 Compact Test Generation for Small-Delay Defects Using Testable-Path Information
Dong Xiang, Boxue Yin, and Krishendu Chakrabarty

9B-4 At-Speed Scan Test Method for the Timing Optimization and Calibration
Kun-Han Tsai, Ruifeng Guo, and Wu-Tung Cheng

Session 9C: Defect-Based Testing

Time: 10:40 pm - 12:00 pm, Thursday, Nov. 26, 2009

Place: Auditorium

Chair: *Ilia Polian, University of Freiburg, Germany*

9C-1 M-IVC: Using Multiple Input Vectors to Minimize Aging-Induced Delay
Song Jin, Yinhe Han, Lei Zhang, Huawei Li, Xiaowei Li, and Guihai Yan

9C-2 Analysis of Resistive Bridging Defects in a Synchronizer
Hyoung-Kook Kim, Wen-Ben Jone, Laung-Terng Wang, and Shianling Wu

9C-3 On-Chip TSV Testing for 3D IC before Bonding Using Sense Amplification
Po-Yuan Chen, Cheng-Wen Wu, and Ding-Ming Kwai

9C-4 Test Pattern Selection for Potentially Harmful Open Defects in Power Distribution Networks
Yubin Zhang, Lin Huang, Feng Yuan, and Qiang Xu

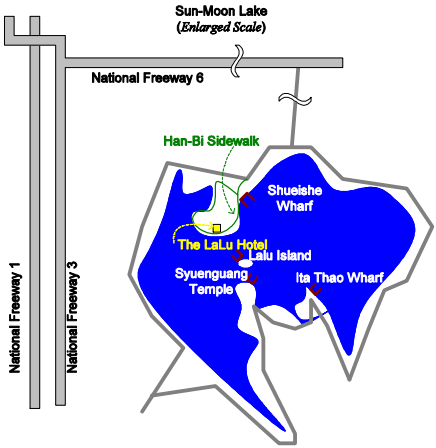
Social Program

Nov. 25, 2009, 1:30 pm - 8:00 pm, Sun Moon Lake, Nantou

The social program at the Eighteenth Asian Test Symposium provides not only the opportunities for informal technical discussions among participants but also a good time for all of our friends. It is our pleasure to invite you to enjoy the banquet with the social program. Please refer to the following schedule, the social program will be held in the most famous and beautiful resort of the middle Taiwan – Sun Moon Lake. After four-hour tour we will enjoy our banquet in the Lalu Hotel. Welcome to the Eighteenth Asian Test Symposium again.

Schedule

Time	Venue
13:30~13:40	1. Gather in **1F Lobby**, Evergreen Laurel Hotel, Taichung 2. Take bus to **Sun Moon Lake**
15:00 ~17:00	1. **Yachting Journey** on Sun Moon Lake 2. Yachting Route**: Shueishe Wharf → Lalu Island → Syuenguang Temple → Ita Thao Wharf → Shueishe Wharf** (http://www.sunmoonlake.gov.tw/EN/02000477.aspx)
17:00~17:30	Lakeside walk
17:30~19:30	Conference **Banquet** in the **LaLu**
19:30~20:00*	Back to **Evergreen Laurel Hotel**, Taichung (Gather in the entrance of the LaLu) *Note: Adjusted by banquet ending time.



Tour – *Sun Moon Lake*

Sun Moon Lake, situated in Nantou County's Yuchih Township, in the center of Taiwan, and is the island's largest lake. It is a beautiful alpine lake, divided by the tiny Lalu Island; the eastern part of the lake is round like the sun and the western side is shaped like a crescent moon, hence the name "Sun Moon Lake". Its crystalline, emerald green waters reflect the hills and mountains which rise on all sides. Natural beauty is enhanced by numerous cultural and historical sites. Well-known both at home and abroad, the Sun Moon Lake Scenic Area has exceptional potential for further growth and recognition as a prime tourism destination. When you visit Sun Moon Lake, we provide 1.5hr travel arrangement by boat. You will have an irresistible impulse to reach the center of the lake, and to come close to the natural beauty of the lakes and mountains.

Banquet – *The Lalu*

The Lalu is located on Sun Moon Lake's Lalu Peninsula. In the past, the building served as Chiang Kai Shek's travel accommodation. The Lalu's architectural design centres on the themes of utmost simplification of Zen style and is constructed with four major building materials of wood, stone, glass and iron. Its unique "Ongoing Style" of architecture has impressed the public and already becomes a model imitated by restaurants, hotels and various personal and business establishments.

Classical Chinese Music

The Zheng, commonly known as Guzheng, is a plucked string instrument that is part of the zither family. It is one of the most ancient Chinese musical instruments according to the documents written in the Qin dynasty (before 206 BC). Zheng is the forerunner of Japanese koto, Korean kayagum, Mongolian yatag, and Vietnamese dan tranh.

Puppet Show

Taiwanese glove puppetry is a drama that is deeply embedded in Taiwanese folk society. In a different era, it served as the Taiwanese people's best outlet for recreation and relaxation. Today, though no longer Taiwan's most important drama activity, glove puppetry continues to adjust to changing trends to offer a glamorous and appealing drama.

Author Index

Welcome to Taichung

Taichung City is located in the middle part of Taichung Basin in central Taiwan. It faces Taiwan Strait in the west and mountains in the east. Taichung City is the third largest city in Taiwan. It is also nicknamed cultural city due to its prosperous cultural activities. Its mild spring-like climate lasts all year long. Hence, it is widely regarded as the best city to live in Taiwan. Art, culture, and educational activities are affluent in Taichung City, such as National Museum of Natural Sciences, National Museum of Fine Arts, Taichung Park, Jhongcheng Park, Fengle Sculpture Park, Taichung Metropolitan Park, etc.

Useful Websites:

Taichung City Government:	http://www.taichung.gov.tw/english
Taichung Travel Net:	http://travel.tccg.gov.tw/english
Evergreen Laurel Hotel:	http://www.evergreen-hotels.com
The Lalu Hotel:	http://www.thelalu.com.tw
National Museum of Natural Sciences:	http://www.nmns.edu.tw
ATS'09 Website:	http://ats09.nchu.edu.tw

Language

Mandarin is the official language in the Republic of China, though other dialects are also spoken. The most commonly used foreign language is English. Taxi drivers, however, generally only speak Mandarin or Taiwanese.

Climate

Taiwan's climate is subtropical with average annual temperatures of 19℃ (66℉) in the north and 21℃ (69℉) in the south. Autumn from September through November, is usually cool with an average temperature from 20℃ to 24℃ (68℉ to 75℉). The weather report of Taiwan can be found at the website of Central Weather Bureau: http://www.cwb.gov.tw

Time Zone

Taiwan is eight hours ahead of Greenwich Mean Time (GMT+8) and does not practice daylight saving time during summer.

Electricity Power Supply

The utility power supply used in Taiwan is 110 volts/60 Hz. Appliances from Europe, Australia or South-East Asia will require an adaptor and/or transformer.

Currency

Taiwan's currency is the New Taiwan Dollar (NT$). Bill denominations are NT$2,000, NT$1,000, NT$500, NT$200, and NT$100. Coin denominations are NT$1, NT$5, NT$10, NT$20, and NT$50. The exchange rate is around NT$32 to US$1. Foreign currencies can be exchanged at the airport upon arrival, or at government-authorized banks, tourist hotels, and department stores. Please retain the currency exchange receipt to exchange unused NT Dollars back to original currency. Traveler's checks in major currencies may be cashed at some tourist-oriented businesses and most international tourist hotels.

Credit Card

Major credit cards are accepted by hotels, department stores, airlines, most stores and restaurants. Cash can be withdrawn from the ATM which has the same logo on your cards. Cash is generally preferred in most places in Taiwan.

Telecommunication Service

A single local call from a public phone costs NT$1 for 3 minutes with additional coins insertion for continuing service. If needed, the overseas operator may be reached by dialing "100". Direct internatinal call is available from some phones, after dialing the prefix “002”. Rate for direct international calls is charged every six seconds.

Customs

Personal items are free of duty. Visitors over 20 years old may bring in, duty free, 200 cigarettes or 25 cigars or 0.5 kg of tobacco, one bottle of liquor and one used camera. Gold cannot be exported without a permit issued by the Ministry of Finance. Passengers arriving with gold and silver and planning to take it out at departure must declare it and leave the items with Customs until they leave Taiwan.

Helpful Phone Numbers

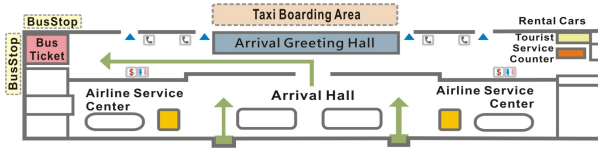
English Speaking Police:	(02)2555-4275 or (02)2556-6007
Emergencies/Fire Department:	119
Police:	110
English Speaking Directory Assistance:	106
International Operator Assistance:	100
Taichung Foreign Affairs Police Station:	(04)2222-3725

Transportation

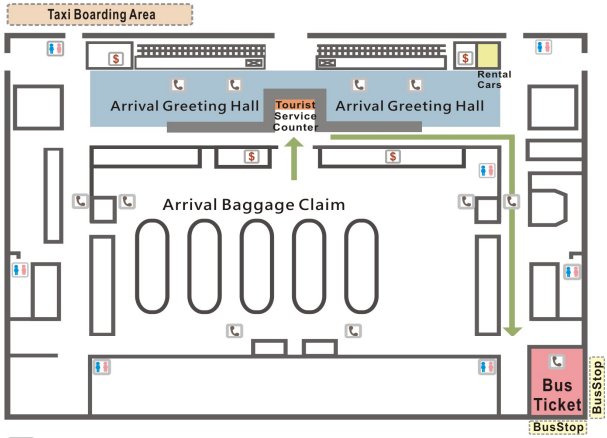
From Taiwan Taoyuan (CKS) Airport

Bus line		Fe Go Express (飛狗巴士)	Kuokuang Line, Taiwan Bus Corp. (國光客運)
Looks			
Service hours	Airport	06:00-01:30	06:30-22:30
	Taichung	02:00-22:00	05:00-18:20
Trip duration		130 mins	130 mins
Bus Stop		Evergreen Laurel Hotel	Chung-Ming Elementary School
Ticket price	Adult	NT$220	NT$220
	Child	NT$190	NT$145
Ticket counters		Arrival Passenger Reception Areas of both Terminals	

Terminal 1: 1st Floor



Terminal 2: 1st Floor



Telephone

Currency Exchange

Toilet

Taiwan High Speed Railway (THSR)

Step1. *Shuttle Bus from Airport to THSR Taoyuan Station*

Bus line:	Ubus 705 line	
Service hours:	Taiwan Taoyuan Airport Terminal 1	(06:30-22:30)
	THRS Taoyuan Station	(07:00-23:45)
Trip duration:	15 mins	
Ticket price:	Adult NT$30; Child NT$15	

Step2. *Taiwan High Speed Railway to Taichung*

Service hours:	THRS Taoyuan Station	(06:52-23:22)
	THRS Taichung Station	(06:30-22:54)
Trip duration:	38 mins	
Station:	THRS Taichung Station	
Ticket price:	Stand Class:	Adult NT$540; Child NT$270
	Business Class:	Adult NT$805; Child NT$505
	Non-reserved:	Adult NT$455; Child NT$250
Timetable:	http://www.thsrc.com.tw/en/	

Step3. *Taxi from THSR Taichung Station to Evergreen Laurel Hotel*

Service hours:	06:00-24:00
Trip duration:	20~30 mins
Charge:	Typical taxi fare to Evergreen Laurel Hotel is approx. NT$250.

In Taichung City

Driving

Get off at the Taichung Chung Kang Rd. interchange from National Rd#1, and drive toward Taichung, and in approximately 2 kilometers you will get off at Evergreen Laurel Hotel (Taichung).

Mass Transit

Get off at Taichung Railway Station from the Taiwan Railway and then get on routes 27, 106 or 88 of Taichung Passenger Service then get off at Station Hecuo.

Get off at Taichung Station from the Taiwan High Speed Rail and get on Ubus85 to the intersection of Wenxin Rd. and Chung Kang Rd. then transfer to Ubus83 you will get off at Evergreen Laurel Hotel (Taichung).

Please take me to the Evergreen Laurel Hotel.

請帶我到台中長榮桂冠酒店

台中市台中港路二段 6 號

Program at a Glance

Date	Time	Program		
Nov. 23 (Mon.)	09:00-12:00	**Tutorial 1**		
	14:00-17:00	**Tutorial 2**		
	18:30-21:00	**Welcome Reception**		
Nov. 24 (Tue.)	09:00-10:20	**Plenary Session 1**		
	10:20-10:40	***Coffee Break***		
	10:40-12:00	**Plenary Session 2**		
	12:00-13:10	***Lunch***		
	13:10-14:30	**3A:** BIST	**3B:** Fault Diagnosis	**3C:** Analog and Mixed-signal Testing
	14:30-14:45	*Coffee Break*		
	14:45-16:05	**4A:** Industrial Session	**4B:** Low-Power Testing	**4C:** On-Line Testing and Silicon Debug
	16:05-16:20	*Coffee Break*		
	16:20-17:40	**5A:** Delay Testing	**5B:** Test Generation I	**5C:** System Test
Nov. 25 (Wed.)	09:00-10:20	**6A:** Panel Session I	**6B:** DFT	**6C:** RF & Analog Testing
	10:20-10:40	***Coffee Break***		
	10:40-12:00	**7A:** SoC Test	**7B:** Test Generation II	**7C:** Test Data Compression
	11:30-13:30	***Lunch***		
	13:30-18:30	**Social Event**		
	18:30-20:00	***Banquet***		
Nov. 26 (Thu.)	09:00-10:20	**8A:** Panel Session II	**8B:** Fault Modeling & Diagnosis	**8C:** Analog and Mixed-signal Testing
	10:20-10:40	***Coffee Break***		
	10:40-12:00	**9A:** Memory Test	**9B:** Test Generation III	**9C:** Defect-Based Testing

The 18th Asian Test Symposium

November 23-26, 2009

Evergreen Laurel Hotel, Taichung, Taiwan

Advance Program

Sponsored by

IEEE Computer Society Test Technology Technical Council

Co-Sponsored by

National Chung-Hsing University

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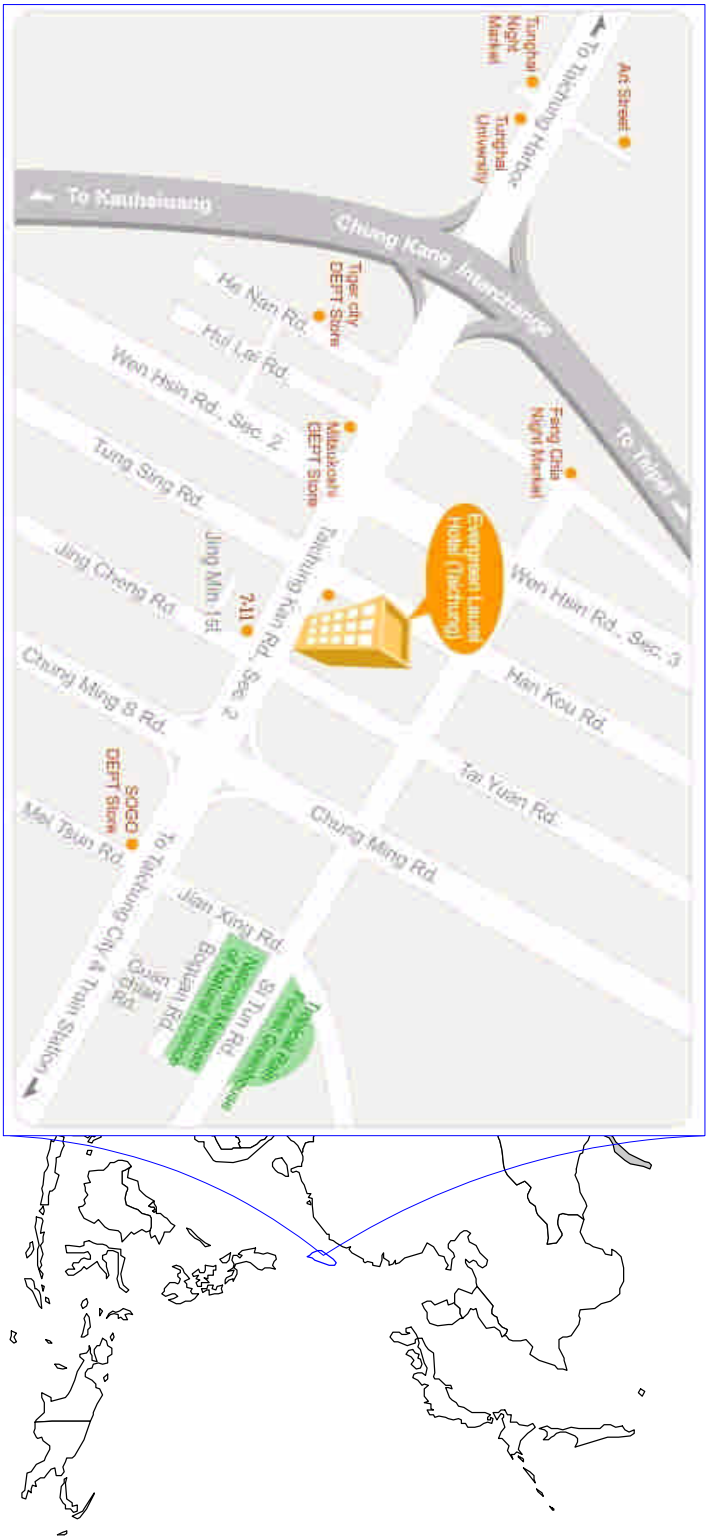

Foreword

Welcome to the Eighteenth Asian Test Symposium (ATS'09). After its debut in Hiroshima, Japan in 1992, the Asian Test Symposium has been held in eighteen cities in Asia and the Pacific Region as the largest symposium that focuses on testing of integrated circuits and systems. Researchers and engineers from all over the world have attended the past symposia and enjoyed discussions. This year the symposium comes to Taichung, Taiwan.

This year, we received 100 technical paper submissions from 16 countries and regions, including 26 from North and South America, 14 from Europe, 26 from Taiwan, seven from Japan, ten from Mainland China, 14 from India, and three from other Asian countries and regions. Each paper was sent to at least three reviewers for evaluation. The program committee meeting was held on July 7, 2009 at the National Chung-Hsing University. Based on the reviewers' rating and comments, 60 regular papers and eight short papers were selected into the final program. The selected papers, which cover nearly all aspects of the key area of VLSI testing, were allocated into 18 technical sessions. We have also selected six industrial papers to form an industry session.

In addition to the technical and industry sessions, the ATS program includes two plenary sessions, two panel sessions and two half-day tutorials. Four keynote addresses in the plenary sessions are given by Professor Niraj K. Jha, Dr. Cheng-Wen Wu, Mr. Sanjiv Taneja and Mr. Erik Jan Marinissen. Two panel sessions are organized by Mr. Anis Uzzaman and Professor Said Hamdioui. Two half-day tutorials are offered in cooperation with the Test Technology Test Education Program (TTEP) of IEEE Computer Society, Test Technology Technical Council (TTTC). One is on low power testing by Dr. Patrick Girard, Dr. Nicola Nicolici, and Dr. Xiaoqing Wen and the other is on system-in-package test by Dr. Yervant Zorian.

Finally we would like to thank the reviewers, the program committee members, the organizing committee members, and the ATS Steering Committee members. We sincerely hope that you will find this event pleasant and enlightening.

Welcome to Taichung and enjoy ATS'09!

General Co-chairs
Shi-Yu Huang, *National Tsing Hua University*
Ming-Der Shieh, *National Cheng Kung University*

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Sying-Jyan Wang, *National Chung-Hsing University*

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North American Liaison

Alex Orailoglu, *University of California at San Diego, USA*

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Seongmoon Wang
Hung-Pin Wen
Xiaoqing Wen
Yun-Che Wen
Chin-Long Wey
Cheng-Wen Wu
Wen-Ching Wu
Dong Xiang

Tutorials

Tutorial I

Power-Aware Testing and Test Strategies for Low Power Devices

9:00 am -12:00 pm, Monday, Nov. 23, Auditorium

Patrick Girard, *LIRMM/CNRS*
Nicola Nicolici, *McMaster University*
Xiaoqing Wen, *Kyushu Institute of Technology*

Summary: Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability.

Tutorial II

System-in-Package Test Strategies

13:30 pm -16:30 pm, Monday, Nov. 23, Auditorium

Yervant Zorian, *Virage Logic Corp*

Summary: Today's miniaturization and performance requirements result in the usage of high density advanced packaging technologies, such as System-in-Package (SiP), 3D integration, Direct Chip Attach, Package-in-package. Due to their physical access limitation, the complexity and cost associated with their test and diagnosis are considered major issues facing their use. This tutorial provides comprehensive knowledge of test solutions for advanced packages by placing particular emphasis on: test and debug approaches for bare dies; testing schemes for 3D packages, flip-chips used in direct chip attach, and SiP packages; testing bare substrates, and finally test, diagnosis and repair techniques for assembled modules.

Plenary Sessions

Opening Remarks

9:00 am - 9:20 am, Tuesday, Nov. 24, Evergreen Ballroom

Shi-Yu Huang, *General Co-chair*
Ming-Der Shieh, *General Co-chair*
Sying-Jyan Wang, *Program Chair*

Keynote Speech I

Testing Challenges for Emerging Nanotechnologies

9:20 am - 9:55 am, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Niraj K. Jha, *Princeton University, USA*

Chair: Chin-Long Wey, *National Chip Implementation Center, Taiwan*

Summary: The march to miniaturization of semiconductor technology continues. However, Moore's Law does take a toll on Testing Engineers by making manufacturing-time testing ever more difficult. As if the testing challenges posed by the continued CMOS miniaturization were not enough, recognizing that CMOS is approaching its physical limits, new nanotechnologies are emerging with novel logic primitives that pose several new challenges in fault modeling, test generation, fault simulation, and design for testability. This talk will begin with some of the testing challenges posed by current CMOS technology. Power-aware test has a rich history. However, we will show that temperature-aware test and power-aware test are not necessarily the same. Thus, a similar concerted effort is necessary for developing temperature-aware test techniques. Then we will move on to the test challenges posed by double-gate CMOS technology, such as FinFETs, which are expected to bridge the gap till the 10nm technology node as single-gate CMOS runs out of steam. Temperature-aware test will be even more important for FinFETs. Several nanotechnologies are vying to take us beyond the 10nm technology node, such as resonant tunneling diodes, quantum cellular automata, nanowires, nanotubes, graphene, single electron transistors, quantum computing, etc. We will finally discuss the testing challenges posed by some of these nanotechnologies.

Keynote Speech II

Wireless Testing and 3D Integrated Devices: Can They Save Our Jobs?

9:55 am - 10:30 am, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Cheng-Wen Wu, *ITRI, Taiwan*

Chair: Kuen-Jong Lee, *National Cheng Kung University, Taiwan*

Summary: Testing has contributed a significant portion of the cost in manufacturing advanced semiconductor products. To address this issue, we have proposed the HOY test system, which features wireless communication and enhanced embedded test circuits. In this talk, we first provide the concept, architecture, and test flow for future semiconductor products tested by HOY. We then discuss in detail the testing of embedded memories and logic blocks by HOY. A prototype system has been developed and experimental results will be shown. Another thought is about the development cost of a typical system-on-chip (SOC) using state-of-the-art technology---tens of million dollars for a case, and the cost continues to soar with the ever innovating technology. Today, more and more people are thinking about turning to three-dimensional (3D) integration for possible alternatives that provide better or equal performance with lower cost. Stacking dies using the Through-Silicon-Via (TSV) technology has been considered one of the most promising solutions to extending the life of Moore's Law in semiconductor industry, but of course there are problems to be solved before the infrastructure can be set up to support the industry for manufacturing TSV-based 3D integrated devices. In this talk we will also discuss the design and test issues, and possible solutions for 3D integrated devices. A link between HOY and 3D-IC testing will be established as well.

Keynote Speech III

Can Innovations in Test Serve as a Beacon of Light in a Dark Economy?

10:50 am -11:25 am, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Sanjiv Taneja, *Cadence Design Systems, USA*

Chair: Shi-Yu Huang, *National Tsing Hua University Taiwan*

Summary: While it is widely accepted that R&D innovations serve as the growth engine to gain market share and drive profitability in technology business, tough economic times present some big challenges to that premise. The first challenge is how to innovate when R&D budgets are tight and funding for new breakthrough ideas is limited. The second challenge -- specific to manufacturing test -- is that the true value of Test is cloaked under the myth of "high Cost of Test" leading some semiconductor businesses to stray away from adequate levels of investment that is needed to maintain the quality levels and withstand increasingly fierce competition in the era of economic globalization. Another challenge relates to linking innovation to business strategies when the short-term considerations become a barrier to moving the innovation process forward.

In this talk, we will address some of the solutions to these challenges by drawing upon real life experiences in the area of DFT/ATPG/Diagnostics in a corporate setting. The solutions range from managing innovation with a similar degree of discipline that gets applied to the rest of the business operations, creating an innovation-centric corporate environment, collaborating with customers and universities on high impact problems and creating the sparks of imagination that fuel the innovation process to focusing on rapidly transforming the innovations to complete solutions that meet customers' needs and maximize the return on investment.

Keynote Speech IV

Challenges and Solutions for Testing TSV-Based 3D-SICs

11:25 am -12:00 pm, Tuesday, Nov. 24, Evergreen Ballroom

Speaker: Erik Jan Marinissen, *IMEC, Belgium*

Chair: Ming-Der Shieh, *National Cheng Kung University, Taiwan*

Summary: Three-dimensional stacked ICs (3D-SICs) offer dense integration of possibly heterogeneous technologies at a small footprint. Interconnection of the various tiers by means of Through-Silicon Vias (TSVs) promises to increase the interconnect bandwidth and performance while lowering power dissipation and manufacturing cost, and hence might help the semiconductor industry to extend the momentum of Moore's Law into the next decade. Testing for manufacturing defects is considered by many as a major, still largely unresolved obstacle to make 3D integrated circuits a reality. It is regarded as the "No. 1 Challenge" among all challenges for 3D-SICs (Keynote Speech at the 2007 3D Architecture Conference by Ted Vucurevich, former CTO of Cadence Design Systems). There are concerns about testing cost, and even the feasibility of testing such TSV-based 3D-SICs. In this presentation, after a review of TSV-based technologies, we present a structured overview of the challenges in testing 3D-SICs, along with solutions as far as available today. Whereas these 'super chips' require most of today's advanced test and DfT approaches, they also have some unique challenges of their own. These include (1) development of new fault models and corresponding tests for thinned-die defects and TSV-based interconnects, (2) wafer probing on small and numerous micro-bumps and/or TSV tips under stringent damage requirements, (3) handling of and probing on wafers with thinned-die stacks, (4) further strengthening of the well-known modular test concept, (5) the design, partitioning, and optimization of DfT architectures that span across multiple dies, and (6) optimization of the test flow for maximum effectiveness and lowest cost.

Panel Discussions

Panel Session I

Is Low Power Testing Necessary?
What does the Test Industry Truly Need?
Real Issues and Available Solutions

9:00 am -10:20 am, Wednesday, Nov. 25, Laurel Salon I

Organizer/Moderator: Anis Uzzaman – *Cadence Design Systems, Inc., USA*

Potential Panelists: Xiaoqing Wen –*Kyushu Institute of Technology, Japan*
Kazumi Hatayama – *STARC, Japan*
Sanjiv Taneja – *Cadence Design Systems, Inc., USA*
Erik Jan Marinissen – *IMEC, Belgium*

Abstract: With the changing face of the consumer driven semiconductor industry, there are new challenges facing the industry which need to be resolved. Minimizing Power dissipation is a significant and growing challenge with the growth of the wireless and portable device segments and with the need to be 'green'. Even during manufacturing test, power is definitely among the top ten items needing attention and expertise. Since 90-nm there has been a recognition that power consumption during test can be a factor affecting product quality and yield. Excessive power consumption during manufacturing test affects the reliability of digital integrated circuits, leading to power-driven failures and higher infant mortality. These trends if continuing on their present course will force designers to adopt specific power management and low power design techniques for manufacturing test.

Power consumption during functional operation is no longer the only area of concern. Power is increasingly becoming an issue during various manufacturing test modes of the circuit operation. It has been found in several studies that the normal scan test mode power consumption is several times higher than the functional power consumption in existing designs. While typical test mode power consumption limits are usually around 2X functional power, field testing requires test power to be as low as worst-case functional power. Also, burn-in test and high-voltage testing of chips becomes more difficult as power consumption increases significantly with elevated voltages and temperatures.

There are several reasons why test power is higher than functional power. One of the reasons is that during the test phase simultaneous testing of multiple modules is done to reduce test costs in general. This might not necessarily be true during functional operation. Redundant switching in circuit logic during scan shift and unduly high switching during scan shift/capture also adds up to the high power consumption of the circuit during test. Higher frequency operation of scan chains during Built-in-self-test (BIST) can also result in more power consumption during test comparing to circuit's functional operation. With at-speed transition fault patterns becoming a necessary component of all test suites supplied to production engineers, fast at-speed capture pulses in scan transition pattern tests can cause undue peak power spikes or IR drop issues. Also, increasing frequency of scan shift as tester supplied clock frequency increases might

be another reason why test operation can consume more power than the functional operation of the circuit.

In an ideal profile for developing and implementing a manufacturing test power reduction strategy, the power reduction effectiveness is expected to be high and usable with on-chip compression. The test coverage impact is also expected to be low and there must be minimum impact on ATPG tools and flows. On the other side, the test data volume and test time should not be impacted by the power reduction strategy. Finally, the strategy must not impact physical design care-abouts and functional timing. Obviously, the power reduction strategy is complex but must not place production at risk.

Various power reduction and power management techniques have been proposed in the literature some of which are deployed in chips manufactured today using commercial low-power design tools. Two such examples of power management techniques are clock gating and power domain partitioning. DFT Insertion is another technique for reducing test power. The combinational circuit toggling that happens during scan shift can be eliminated (reduced) if blocking circuitry can be incorporated at all (some) Q outputs of the scan flip flops. Scan segmentation/partitioning is another DFT technique using which power during test can be controlled.

Low-power scan partitioning has been shown to be feasible on commercial designs such as the CELL processor. Some of the other DFT techniques for reducing test power include data gating, wherein, for a design with modules A and B, test points are added that allow for scan in of zeros into the scan chains of module A, while module B is tested, and vice versa. Staggered Clocking is another method using which test power consumption is controlled today during test in many designs.

Aside from the above mentioned DFT based power reduction techniques, some of the ATPG techniques are also used for reduced power consumption; intelligent care bit filling has been known as one of the effective methods to gain considerable reduction in power consumption. Various X-fill techniques have been proposed in the literature including 0-fill, adjacent fill, repeat fill, preferred fill, and so on. Another item that should also be given serious thought is the testing of the power management circuitry – power controller, power switches, retention flops, etc. – that is inserted for the functional power control. In many cases, the power management components themselves are overlooked during manufacturing test, there are many questions as how to test the new power management/reduction structures, how to handle these structures while testing the rest of the chip and how to leverage these structures when testing multiple power domains.

With so many open options available for power reduction during test, it is still very difficult to identify the right technique to use for a certain technology device. Also, it is still difficult to identify any power related issue during testing as it is typically identified through prediction and analysis at the ATE. In addition, with all the low power standardization going on in the test industry, it is very confusing for a designer on which standard to follow and adopt.

Some of the major questions that can be the focus of discussion during this panel session are:

- How much of low power issues the test industry is experiencing today?
- Is "POWER DURING TEST" really an issue or just a rumor? If this is a reality then for what process technology we are seeing this to be an issue?
- Is there any easy way to isolate the low power issue occurring during test? What are the specific symptoms?
- What are the measures that people take in general for handling the low power issues today?
- What are the future "TO DOs" in the area of lower geometry technologies.

The objective of this panel is to provide a comprehensive understanding of the power problem during test, outline the various challenges involved, and discuss various existing and emerging solutions to tackle them.

Panel Session II

Testing Embedded Memories in the Nano-Era: Will the existing approaches survive?

9:00 am -10:20 am, Thursday, Nov. 26, Laurel Salon I

Organizer/Moderator: Said Hamdioui, *Delft Univ. of Technology, Netherlands*

Panelists:
Jin-Fu Li – National Central University, Taiwan
Ting-Pu Tai – Mentor Graphics, USA
Ad. J. van de Goor – ComTex/TUDelft, the Netherlands
Cheng-Wen Wu – National Tsing Hua University, Taiwan
Shianling Wu – SynTest Technologies, USA

Summary:

Embedded memories have become the fastest growing segment of Systems on Chip (SoC) in recent years. According to the International Technology Roadmap for Semiconductors, embedded memories will continue to dominate the increasing SoC chip area in the future, approaching 94% within one decade. Hence, these memories will severely impact all aspects of SoC manufacturing including yield, quality and reliability. Additionally, nano-technology is causing higher levels of device-parameter variations and new failure mechanisms that are not yet fully understood. Consequently, the existing fault models and test approaches may be not adequate to test embedded memories in the nano-era. Therefore, a radical paradigm change may be needed.

The panel aims at gathering opinions on the different ways to deal with test challenges of embedded memories in the nano-era. The main question is how to deal with this shift in failure mechanisms in order to keep an acceptable product quality at affordable cost. Can the existing test approaches do the job? Do we need to rely more on stresses rather than the algorithms themselves? However, too much stress/ Burn-in may degrade the lifetime of the chip. Do we need to move more towards DFT rather than March tests? Is programmable DFT the ideal solution? Can on-the-fly detect/repair and reconfigure be the answer? Or do we need completely new approaches?

On-Site Registration

Payment: Only credit card or cash will be accepted.

Place: Hallway in Level B2, Evergreen Laurel Hotel, Taichung

Time: Tutorials 09:00 am - 05:00 pm, Nov. 23

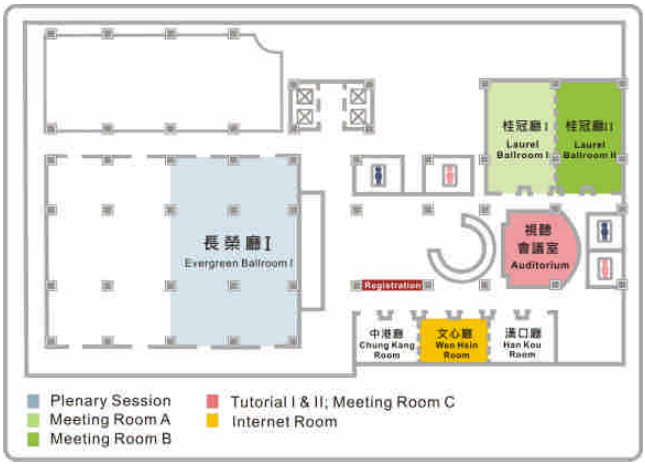
Symposium 08:00 am - 05:00 pm, Nov. 24
08:00 am -12:00 pm, Nov. 25
08:00 am -12:00 pm, Nov. 26

Hotel Information

The Evergreen Laurel Hotel Taichung is offering special rates to attendees of the ATS 09 in Taichung. The number of budget rooms is limited and is on a first-come-first-serve basis. The reservation form can be downloaded from http://ats09.nchu.edu.tw.

Site Map

Level B2, Evergreen Laurel Hotel, Taichung



Technical Paper Sessions

Session 3A: Built-In Self-Test

Time: 13:10 pm - 14:30 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon I

Chair: *Yinhe Han, Chinese Academy of Sciences, China*

3A-1 CA Based Built-In Self-Test Structure for SoC
Sukanta Das and Biplab K. Sikdar

3A-2 A Random Jitter RMS Estimation Technique for BIST Applications
Jae Wook Lee, Ji Hwan Chun, and Jacob A. Abraham

3A-3 A Novel Seed Selection Algorithm for Test Time Reduction in BIST
Rupsa Chakraborty and Dipanwita Roy Chowdhury

3A-4 Logic BIST Architecture for System-Level Test and Diagnosis
Jun Qian, Xingang Wang, Qinfu Yang, Fei Zhuang, Junbo Jia, Xiangfeng Li, Yuan Zuo, Jayanth Mekkoth, Jinsong Liu, Hao-Jan Chao, Shianling Wu, Huafeng Yang,Lizhen Yu, FeiFei Zhao, and Laung-Terng Wang

Session 3B: Fault Diagnosis

Time: 13:10 pm - 14:30 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon II

Chair: *Xiaoqing Wen, Kyushu Institute of Technology, Japan*

3B-1 Fault Diagnosis under Transparent-Scan
Irith Pomeranz and Sudhakar M. Reddy

3B-2 Scan Chain Diagnosis by Adaptive Signal Profiling with Manufacturing ATPG Patterns
Yu Huang, Wu-Tung Cheng, Ruifeng Guo, Ting-Pu Tai, Feng-Ming Kuo, and Yuan-Shih Chen

3B-3 On Improving Diagnostic Test Generation for Scan Chain Failures
Xun Tang, Ruifeng Guo, Wu-Tung Cheng, Sudhakar M. Reddy, and Yu Huang

3B-4 On Scan Chain Diagnosis for Intermittent Faults
Dan Adolfsson, Joanna Siew, Erik Jan Marinissen, and Erik Larsson

Session 3C: Analog and Mixed-Signal Testing I

Time: 13:10 pm - 14:30 pm, Tuesday, Nov. 24, 2009

Place: Auditorium

Chair: *Hao-Chiao Hong, National Chiao Tung University, Taiwan*

3C-1 Design-for-Test Circuit for the Reduced Code Based Linearity Test Method in Pipelined ADCs with Digital Error Correction Technique
Jin-Fu Lin, Soon-Jyh Chang, and Chih-Hao Huang

3C-2 Multi-tone Testing of Linear and Nonlinear Analog Circuits Using Polynomial Coefficients
Suraj Sindia, Virendra Singh, and Vishwani D. Agrawal

3C-3 Low Cost Dynamic Test Methodology for High Precision ΔΔ ADCs
S. Kook, Hyun Choi, Vishwanath Natarajan, Abhijit Chatterjee, Alfred Gomes, Shalahb Goyal, and Le Jin

3C-4 Very-Low-Voltage Testing of Amorphous Silicon TFT Circuits
Shiue-Tsung Shen, Wei-Hsiao Liu, En-Hua Ma, James Chien-Mo Li, and I-Chun Cheng

Session 4A: Industrial Session

Time: 14:45 pm - 16:05 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon I

Chair: *Wu-Tung Cheng, Mentor Graphics Corporation, USA*

4A-1 Scan Compression Implementation in Industrial Design - Case Study
Dragon Hsu and Ron Press

4A-2 Calibration as a Functional Test: An ADC Case Study
Hsiu-Ming Chang, Kuan-Yu Lin, and Kwang-Ting Cheng

4A-3 Customized Algorithms for High Performance Memory Test in Advanced Technology Node
Shomo Chen, Ning Huang, Ting-Pu Tai, and Actel Niu

4A-4 A Practical DFT Approach for Complex Low Power Designs
Augusli Kifli, Y.W. Chen, Y.W. Tsay, and K.C. Wu

4A-5 DFT Challenges in Next Generation Multi-media IP
Mukund Mittal, Subrangshu Das, and S. Vishwanath

4A-6 Yield Ramp up by Scan Chain Diagnosis
Feng-Ming Kuo and Yuan-Shih Chhen

Session 4B: Low-Power Testing

Time: 14:45 pm - 16:05 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon II

Chair: *Patrick Girard, LIRMM, France*

4B-1 CAT: A Critical-Area-Targeted Test Set Modification Scheme for Reducing Launch Switching Activity in At-Speed Scan Testing
K. Enokimoto, X. Wen, Y. Yamato, K. Miyase, H. Sone, S. Kajihara, M. Aso, and H. Furukawa

4B-2 New Scheme of Reducing Shift and Capture Power Using the X-Filling Methodology
Tsung-Tang Chen, Wei-Lin Li, Po-Han Wu, and Jiann-Chyi Rau

4B-3 Deterministic Built-In Self-Test Using Multiple Linear Feedback Shift Registers for Low-Power Scan Testing
Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chi-Wei Yu

Session 4C: On-Line Testing and Silicon Debug

Time: 14:45 pm - 16:05 pm, Tuesday, Nov. 24, 2009

Place: Auditorium

Chair: *Chih-Tsun Huang, National Tsing Hua University, Taiwan*

4C-1 Low Overhead Time-Multiplexed Online Checking: A Case Study of An H.264 Decoder
Ming Gao and Kwang-Ting Cheng

4C-2 A FPGA-Based Reconfigurable Software Architecture for Highly Dependable Systems
Stefano Di Carlo, Paolo Prinetto, and Alberto Scionti

4C-3 Using Non-trivial Logic Implications for Trace Buffer-Based Silicon Debug
Sandesh Prabhakar and Michael Hsiao

4C-4 A Post-Silicon Debug Support Using High-Level Design Description
Yeonbok Lee, Tasuku Nishihara, Takeshi Matsumoto, and Masahiro Fujita

Session 5A: Delay Testing

Time: 16:20 pm - 17:40 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon I

Chair: *Jing-Jia Liou, National Tsing Hua University, Taiwan*

5A-1 A Low Overhead On-Chip Path Delay Measurement Circuit
Songwei Pei, Huawei LI, and Xiaowei LI

5A-2 An Adaptive Test for Parametric Faults Based on Statistical Timing Information
Michihiro Shintani, Takumi Uezono, Tomoyuki Takahashi, Hiroyuki Ueyama, Takashi Sato, Kazumi Hatayama, Takashi Aikyo, and Kazuya Masu

5A-3 A Delay Measurement Technique Using Signature Registers
Kentaroh Katoh, Toru Tanabe, Haque Md Zahidul, Kazuteru Namba, and Hideo Ito

5A-4 Functional Built-In Delay Binning and Calibration Mechanism for On-Chip at-Speed Self Test
Chen-I Chung, Jyun-Sian Jhou, Ching-Hwa Cheng, and Sih-Yan Li

Session 5B: Test Generation I

Time: 16:20 pm - 17:40 pm, Tuesday, Nov. 24, 2009

Place: Laurel Salon II

Chair: *James Chien-Mo Li, National Taiwan University, Taiwan*

5B-1 A Practical Approach to Threshold Test Generation for Error Tolerant Circuits
Hideyuki Ichihara, Kenta Sutoh, Yuki Yoshikawa, and Tomoo Inoue

5B-2 Speeding up SAT-Based ATPG Using Dynamic Clause Activation
Stephan Eggersglüß, Daniel Tille, and Rolf Drechsler

5B-3 N-distinguishing Tests for Enhanced Defect Diagnosis
Gang Chen, Janusz Rajski, Sudhakar Reddy, and Irith Pomeranz

5B-4 Dynamic Compaction in SAT-Based ATPG
Alexander Czutro, Ilia Polian, Piet Engelke, Sudhakar M. Reddy, and Bernd Becker

Session 5C: System Test

Time: 16:20 pm - 17:40 pm, Tuesday, Nov. 24, 2009

Place: Auditorium

Chair: *Yu Huang, Mentor Graphics Corporation, USA*

5B-5 SIRUP: Switch Insertion in RedUndant Pipeline Structures for Yield and Yield/Area Improvement
Mohammad Mirza-Aghatabar, Melvin A. Breuer, and Sandeep K. Gupta

5B-6 Transaction Level Modeling and Design Space Exploration for SOC Test Architectures
Chin-Yao Chang, Chih-Yuan Hsiao, Kuen-Jong Lee, and Alan P. Su

5B-7 Efficient Software-Based Self-Test Methods for Embedded Digital Signal Processors
Jun-Jie Zhu, Wen-Ching Lin, Jheng-Hao Ye, and Ming-Der Shieh

Session 6A: Panel Session I

Time: 9:00 am - 10:20 am, Wednesday, Nov. 25, 2009

Place: Laurel Salon I

Moderator: *Anis Uzzaman, Cadence Design Systems, Inc., USA*

6A-1 Is Low Power Testing Necessary? What does the Test Industry Truly Need?

Session 6B: DFT

Time: 9:00 am - 10:20 am, Wednesday, Nov. 25, 2009

Place: Laurel Salon II

Chair: *Dong Xiang, Tsinghua University, China*

6B-1 A Scalable Scan Architecture for Godson-3 Multicore Microprocessor
Zichu Qi, Hui Liu, Xiangku Li, Da Wang, Yinhe Han, Huawei Li, and Weiwu Hu

6B-2 Kiss the Scan Goodbye: A Non-scan Architecture for High Coverage, Low Test Data Volume and Low Test Application Time
Michael S. Hsiao and Mainak Banga

6B-3 Multiple Scan Trees Synthesis for Test Time/Data and Routing Length Reduction under Output Constraint
Katherine Shu-Min Li, Yu-Chen Hung, and Jr-Yang Huang

6B-4 Leveraging Partially Enhanced Scan for Improved Observability in Delay Fault Testing
Deepak K.G., Robinson Reyna, Virendra Singh, and Adit D. Singh

Session 6C: RF and Analog Testing

Time: 9:00 am - 10:20 am, Wednesday, Nov. 25, 2009

Place: Auditorium

Chair: *Jiun-Lang Huang, National Taiwan University, Taiwan*

6C-1 BIST Driven Power Conscious Post-Manufacture Tuning of Wireless Transceiver Systems Using Hardware-Iterated Gradient Search
Vishwanath Natarajan, Shyam Kumar Devarakond, Shreyas Sen, and Abhijit Chatterjee

6C-2 Self-Calibrating Embedded RF Down-Conversion Mixers
Abhilash Goyal, Madhavan Swaminathan, and Abhijit Chatterjee

6C-3 A BIST Solution for the Functional Characterization of RF Systems Based on Envelope Response Analysis
Manuel J. Barragán, Rafaella Fiorelli, Diego Vázquez, Adoración Rueda, and José L. Huertas

6C-4 Exploiting Zero-Crossing for the Analysis of FM Modulated Analog/RF Signals Using Digital ATE
Nicolas Pous, Florence Azaïs, Laurent Latorre, Pascal Nouet, and Jochen Rivoir

Session 7A: SoC Test

Time: 10:40 am - 12:00 pm, Wednesday, Nov. 25, 2009

Place: Laurel Salon I

Chair: *Erik Jan Marinissen , IMEC, Belgium*

7A-1 IEEE 1500 Compatible Interconnect Test with Maximal Test Concurrency
Katherine Shu-Min Li, Yi-Yu Liao, Yuo-Wen Liu, and Jr-Yang Huang

7A-2 Multiple-Core under Test Architecture for HOY Wireless Testing Platform
ung-Yu Chen, Ying-Yen Chen, Chun-Yu Yang, and Jing-Jia Liou

7A-3 Partition Based SoC Test Scheduling with Thermal and Power Constraints under Deep Submicron Technologies
Chunhua Yao, Kewal K. Saluja, and Parameswaran Ramanathan

7A-4 Test Integration for SOC Supporting Very Low-Cost Testers
Chun-Chuan Chi, Chih-Yen Lo, Te-Wen Ko, and Cheng-Wen Wu

Session 7B: Test Generation II

Time: 10:40 am - 12:00 pm, Wednesday, Nov. 25, 2009

Place: Laurel Salon II

Chair: *Michael Hsiao, Virginia Tech, USA*

7B-1 Why is Conventional ATPG Not Sufficient for Advanced Low Power Designs?
Krishna Chakravadhanula, Vivek Chickermane, Brion Keller, Patrick Gallagher, and Anis Uzzaman

7B-2 New Class of Tests for Open Faults with Considering Adjacent Lines
Hiroshi Takahashi, Yoshinobu Higami, Yuzo Takamatsu, Koji Yamazaki, Toshiyuki Tsutsumi, Hiroyuki Yotsuyanagi, and Masaki Hashizume

7B-3 Test Pattern Selection and Customization Targeting Reduced Dynamic and Leakage Power Consumption
Subhadip Kundu, Krishna Kumar S., and Santanu Chattopadhyay

7B-4 Deterministic Algorithms for ATPG under Leakage Constraints
Görschwin Fey

Session 7C: Test Data Compression

Time: 10:40 am - 12:00 pm, Wednesday, Nov. 25, 2009

Place: Auditorium

Chair: *Kazumi Hatayama, STARC, Japan*

7C-1 Extended Selective Encoding of Scan Slices for Reducing Test Data and Test Power
Jun Liu, Yinhe Han, and Xiaowei Li

7C-2 A Multi-dimensional Pattern Run-Length Method for Test Data Compression
Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chen-Lun Lee

7C-3 Bit-Operation-Based Seed Augmentation for LFSR Reseeding with High Defect Coverage
Hongxia Fang, Krishnendu Chakrabarty, and Rubin Parekhji

Session 8A: Panel Session II

Time: 9:00 am - 10:20 am, Thursday, Nov. 26, 2009

Place: Laurel Salon I

Chair: *Said Hamdioui, Delft Univ. of Technology, Netherlands*

8A-1 Testing Embedded Memories in the Nano-Era: Will the Existing Approaches Survive?
Said Hamdioui

Session 8B: Fault Modeling & Diagnosis

Time: 9:00 am - 10:20 am, Thursday, Nov. 26, 2009

Place: Laurel Salon II

Chair: *Michel Renovell, LIRMM, France*

8B-1 A Non-Intrusive and Accurate Inspection Method for Segment Delay Variabilities
Ying-Yen Chen and Jing-Jia Liou

8B-2 Bridging Fault Diagnosis to Identify the Layer of Systematic Defects
Po-Juei Chen, James Chien-Mo Li, and Hsing Jasmine Chao

8B-3 Delay Fault Diagnosis in Sequential Circuits
Youssef Benabboud, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, and Olivia Riewer

8B-4 A Partially-Exhaustive Gate Transition Fault Model
Brion Keller, Dale Meehl, Anis Uzzaman, and Richard Billings

Session 8C: Analog and Mixed-Signal Testing II

Time: 9:00 am - 10:20 am, Thursday, Nov. 26, 2009

Place: Auditorium

Chair: *Soon-Jyh Chang, National Cheng Kung University, Taiwan*

8C-1 An On-Chip Integrator Leakage Characterization Technique and Its Application to Switched Capacitor Circuits Testing
Chen-Yuan Yang, Xuan-Lun Huang, and Jiun-Lang Huang

8C-2 LFSR-Based Performance Characterization of Nonlinear Analog and Mixed-Signal Circuits
Joonsung Park, Jaeyong Chung, and Jacob A. Abraham

8C-3 A Jitter Characterizing BIST with Pulse-Amplifying Technique
An-Sheng Chao and Soon-Jyh Chang

8C-4 A Low-Cost Output Response Analyzer for the Built-in-Self-Test .-Δ Modulator Based on the Controlled Sine Wave Fitting Method
Shao-Feng Hung, Hao-Chiao Hong, and Sheng-Chuan Liang

Session 9A: Memory Test

Time: 10:40 am - 12:00 pm, Thursday, Nov. 26, 2009

Place: Laurel Salon I

Chair: *Shyue-Kung Lu, National Taiwan University of Science and Technology, Taiwan*

9A-1 New Algorithms for Address Decoder Delay Faults and Bit Line Imbalance Faults
Ad J. van de Goor, Said Hamdioui, Georgi N. Gaydadjiev, and Zaid Al-Ars

9A-2 Testability Exploration of 3-D RAMs and CAMs
Yu-Jen Huang and Jin-Fu Li

9A-3 Fault Diagnosis Using Test Primitives in Random Access Memories
Zaid Al-Ars and Said Hamdioui

Session 9B: Test Generation III

Time: 10:40 pm - 12:00 pm, Thursday, Nov. 26, 2009

Place: Laurel Salon II

Chair: *Hiroshi Takahashi, Ehime University, Japan*

9B-1 Test Generation for Designs with On-Chip Clock Generators
Xijiang Lin and Mark Kassab

9B-2 On the Generation of Functional Test Programs for the Cache Replacement Logic
W. Perez, D. Ravotto, E. Sanchez, M. Sonza Reorda, and A. Tonda

9B-3 Compact Test Generation for Small-Delay Defects Using Testable-Path Information
Dong Xiang, Boxue Yin, and Krishendu Chakrabarty

9B-4 At-Speed Scan Test Method for the Timing Optimization and Calibration
Kun-Han Tsai, Ruifeng Guo, and Wu-Tung Cheng

Session 9C: Defect-Based Testing

Time: 10:40 pm - 12:00 pm, Thursday, Nov. 26, 2009

Place: Auditorium

Chair: *Ilia Polian, University of Freiburg, Germany*

9C-1 M-IVC: Using Multiple Input Vectors to Minimize Aging-Induced Delay
Song Jin, Yinhe Han, Lei Zhang, Huawei Li, Xiaowei Li, and Guihai Yan

9C-2 Analysis of Resistive Bridging Defects in a Synchronizer
Hyoung-Kook Kim, Wen-Ben Jone, Laung-Terng Wang, and Shianling Wu

9C-3 On-Chip TSV Testing for 3D IC before Bonding Using Sense Amplification
Po-Yuan Chen, Cheng-Wen Wu, and Ding-Ming Kwai

9C-4 Test Pattern Selection for Potentially Harmful Open Defects in Power Distribution Networks
Yubin Zhang, Lin Huang, Feng Yuan, and Qiang Xu

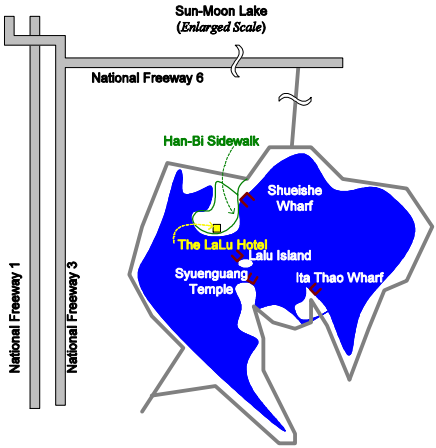
Social Program

Nov. 25, 2009, 1:30 pm - 8:00 pm, Sun Moon Lake, Nantou

The social program at the Eighteenth Asian Test Symposium provides not only the opportunities for informal technical discussions among participants but also a good time for all of our friends. It is our pleasure to invite you to enjoy the banquet with the social program. Please refer to the following schedule, the social program will be held in the most famous and beautiful resort of the middle Taiwan – Sun Moon Lake. After four-hour tour we will enjoy our banquet in the Lalu Hotel. Welcome to the Eighteenth Asian Test Symposium again.

Schedule

Time	Venue
13:30~13:40	1. Gather in **1F Lobby**, Evergreen Laurel Hotel, Taichung 2. Take bus to **Sun Moon Lake**
15:00 ~17:00	1. **Yachting Journey** on Sun Moon Lake 2. Yachting Route**: Shueishe Wharf → Lalu Island → Syuenguang Temple → Ita Thao Wharf → Shueishe Wharf** (http://www.sunmoonlake.gov.tw/EN/02000477.aspx)
17:00~17:30	Lakeside walk
17:30~19:30	Conference **Banquet** in the **LaLu**
19:30~20:00*	Back to **Evergreen Laurel Hotel**, Taichung (Gather in the entrance of the LaLu) *Note: Adjusted by banquet ending time.



Tour – *Sun Moon Lake*

Sun Moon Lake, situated in Nantou County's Yuchih Township, in the center of Taiwan, and is the island's largest lake. It is a beautiful alpine lake, divided by the tiny Lalu Island; the eastern part of the lake is round like the sun and the western side is shaped like a crescent moon, hence the name "Sun Moon Lake". Its crystalline, emerald green waters reflect the hills and mountains which rise on all sides. Natural beauty is enhanced by numerous cultural and historical sites. Well-known both at home and abroad, the Sun Moon Lake Scenic Area has exceptional potential for further growth and recognition as a prime tourism destination. When you visit Sun Moon Lake, we provide 1.5hr travel arrangement by boat. You will have an irresistible impulse to reach the center of the lake, and to come close to the natural beauty of the lakes and mountains.

Banquet – *The Lalu*

The Lalu is located on Sun Moon Lake's Lalu Peninsula. In the past, the building served as Chiang Kai Shek's travel accommodation. The Lalu's architectural design centres on the themes of utmost simplification of Zen style and is constructed with four major building materials of wood, stone, glass and iron. Its unique "Ongoing Style" of architecture has impressed the public and already becomes a model imitated by restaurants, hotels and various personal and business establishments.

Classical Chinese Music

The Zheng, commonly known as Guzheng, is a plucked string instrument that is part of the zither family. It is one of the most ancient Chinese musical instruments according to the documents written in the Qin dynasty (before 206 BC). Zheng is the forerunner of Japanese koto, Korean kayagum, Mongolian yatag, and Vietnamese dan tranh.

Puppet Show

Taiwanese glove puppetry is a drama that is deeply embedded in Taiwanese folk society. In a different era, it served as the Taiwanese people's best outlet for recreation and relaxation. Today, though no longer Taiwan's most important drama activity, glove puppetry continues to adjust to changing trends to offer a glamorous and appealing drama.

Author Index

Welcome to Taichung

Taichung City is located in the middle part of Taichung Basin in central Taiwan. It faces Taiwan Strait in the west and mountains in the east. Taichung City is the third largest city in Taiwan. It is also nicknamed cultural city due to its prosperous cultural activities. Its mild spring-like climate lasts all year long. Hence, it is widely regarded as the best city to live in Taiwan. Art, culture, and educational activities are affluent in Taichung City, such as National Museum of Natural Sciences, National Museum of Fine Arts, Taichung Park, Jhongcheng Park, Fengle Sculpture Park, Taichung Metropolitan Park, etc.

Useful Websites:

Taichung City Government:	http://www.taichung.gov.tw/english
Taichung Travel Net:	http://travel.tccg.gov.tw/english
Evergreen Laurel Hotel:	http://www.evergreen-hotels.com
The Lalu Hotel:	http://www.thelalu.com.tw
National Museum of Natural Sciences:	http://www.nmns.edu.tw
ATS'09 Website:	http://ats09.nchu.edu.tw

Language

Mandarin is the official language in the Republic of China, though other dialects are also spoken. The most commonly used foreign language is English. Taxi drivers, however, generally only speak Mandarin or Taiwanese.

Climate

Taiwan's climate is subtropical with average annual temperatures of 19℃ (66℉) in the north and 21℃ (69℉) in the south. Autumn from September through November, is usually cool with an average temperature from 20℃ to 24℃ (68℉ to 75℉). The weather report of Taiwan can be found at the website of Central Weather Bureau: http://www.cwb.gov.tw

Time Zone

Taiwan is eight hours ahead of Greenwich Mean Time (GMT+8) and does not practice daylight saving time during summer.

Electricity Power Supply

The utility power supply used in Taiwan is 110 volts/60 Hz. Appliances from Europe, Australia or South-East Asia will require an adaptor and/or transformer.

Currency

Taiwan's currency is the New Taiwan Dollar (NT$). Bill denominations are NT$2,000, NT$1,000, NT$500, NT$200, and NT$100. Coin denominations are NT$1, NT$5, NT$10, NT$20, and NT$50. The exchange rate is around NT$32 to US$1. Foreign currencies can be exchanged at the airport upon arrival, or at government-authorized banks, tourist hotels, and department stores. Please retain the currency exchange receipt to exchange unused NT Dollars back to original currency. Traveler's checks in major currencies may be cashed at some tourist-oriented businesses and most international tourist hotels.

Credit Card

Major credit cards are accepted by hotels, department stores, airlines, most stores and restaurants. Cash can be withdrawn from the ATM which has the same logo on your cards. Cash is generally preferred in most places in Taiwan.

Telecommunication Service

A single local call from a public phone costs NT$1 for 3 minutes with additional coins insertion for continuing service. If needed, the overseas operator may be reached by dialing "100". Direct internatinal call is available from some phones, after dialing the prefix “002”. Rate for direct international calls is charged every six seconds.

Customs

Personal items are free of duty. Visitors over 20 years old may bring in, duty free, 200 cigarettes or 25 cigars or 0.5 kg of tobacco, one bottle of liquor and one used camera. Gold cannot be exported without a permit issued by the Ministry of Finance. Passengers arriving with gold and silver and planning to take it out at departure must declare it and leave the items with Customs until they leave Taiwan.

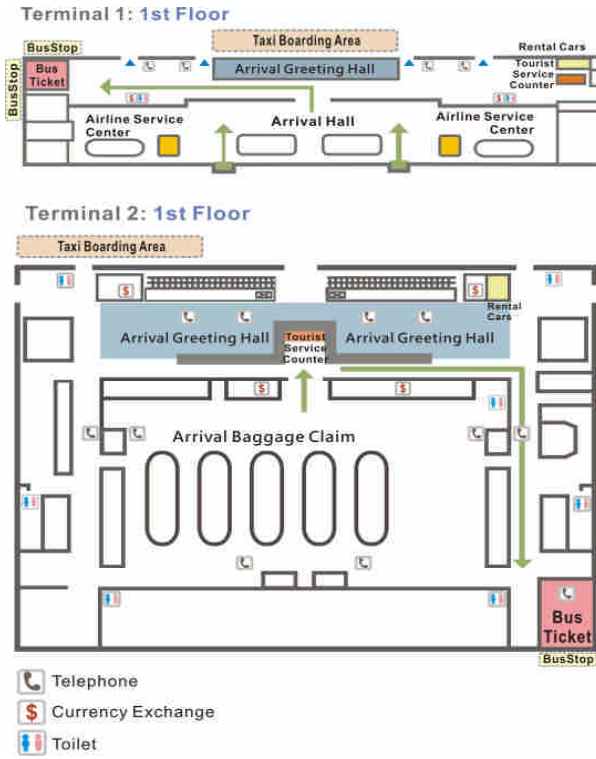
Helpful Phone Numbers

English Speaking Police:	(02)2555-4275 or (02)2556-6007
Emergencies/Fire Department:	119
Police:	110
English Speaking Directory Assistance:	106
International Operator Assistance:	100
Taichung Foreign Affairs Police Station:	(04)2222-3725

Transportation

From Taiwan Taoyuan (CKS) Airport

Bus line		Fe Go Express (飛狗巴士)	Kuokuang Line, Taiwan Bus Corp. (國光客運)
Looks			
Service hours	Airport	06:00-01:30	06:30-22:30
	Taichung	02:00-22:00	05:00-18:20
Trip duration		130 mins	130 mins
Bus Stop		Evergreen Laurel Hotel	Chung-Ming Elementary School
Ticket price	Adult	NT$220	NT$220
	Child	NT$190	NT$145
Ticket counters		Arrival Passenger Reception Areas of both Terminals	



Taiwan High Speed Railway (THSR)

Step1. *Shuttle Bus from Airport to THSR Taoyuan Station*

Bus line:	Ubus 705 line	
Service hours:	Taiwan Taoyuan Airport Terminal 1	(06:30-22:30)
	THRS Taoyuan Station	(07:00-23:45)
Trip duration:	15 mins	
Ticket price:	Adult NT$30; Child NT$15	

Step2. *Taiwan High Speed Railway to Taichung*

Service hours:	THRS Taoyuan Station	(06:52-23:22)
	THRS Taichung Station	(06:30-22:54)
Trip duration:	38 mins	
Station:	THRS Taichung Station	
Ticket price:	Stand Class:	Adult NT$540; Child NT$270
	Business Class:	Adult NT$805; Child NT$505
	Non-reserved:	Adult NT$455; Child NT$250
Timetable:	http://www.thsrc.com.tw/en/	

Step3. *Taxi from THSR Taichung Station to Evergreen Laurel Hotel*

Service hours:	06:00-24:00
Trip duration:	20~30 mins
Charge:	Typical taxi fare to Evergreen Laurel Hotel is approx. NT$250.

In Taichung City

Driving

Get off at the Taichung Chung Kang Rd. interchange from National Rd#1, and drive toward Taichung, and in approximately 2 kilometers you will get off at Evergreen Laurel Hotel (Taichung).

Mass Transit

Get off at Taichung Railway Station from the Taiwan Railway and then get on routes 27, 106 or 88 of Taichung Passenger Service then get off at Station Hecuo.

Get off at Taichung Station from the Taiwan High Speed Rail and get on Ubus85 to the intersection of Wenxin Rd. and Chung Kang Rd. then transfer to Ubus83 you will get off at Evergreen Laurel Hotel (Taichung).

Please take me to the Evergreen Laurel Hotel.

請帶我到台中長榮桂冠酒店

台中市台中港路二段 6 號

The Eighteenth Asian Test Symposium

http://ats09.nchu.edu.tw/
November 23-26, 2009
EVERGREEN LAUREL HOTEL TAICHUNG, Taichung, Taiwan

Registration Form

E-MAIL or FAX this form to: ATS09 Secretariat
E-mail: ats2009.taiwan@gmail.com
Tel: +886-2-8226-1010
Fax: +886-2-8226-2785

Please TYPE or print BLOCK LETTERS and notice the regulations below:
(1) At least one author must register at a non-student rate by **August 10**. Please indicate the paper reference number.
(2) Extra pages fee for each paper exceeding page limit must be paid by **August 10**.
(3) After **October 10**, participating in the social event is not guaranteed.
(4) No registration form will be accepted after **November 6**. After this date, please register on-site.

Name: _____ (Last) _____ (First) _____ (Middle)

Affiliation/company: _____

Mailing address: _____

_____ (Zip/Postal code) _____ (Country) Tel: _____ Fax: _____ E-mail: _____

IEEE membership number: _____ Paper reference number(s): _____ _____ _____

Registration fees (NT Dollar)*[1]	Symposium		Tutorial				Subtotal
			Tutorial 1		Tutorial 2		
	Until Oct. 10	After Oct. 10	Until Oct. 10	After Oct. 10	Until Oct. 10	After Oct. 10	
IEEE member	❑NT$15,000	❑NT$18,000	❑NT$2,350	❑NT$3,000	❑NT$2,350	❑NT$3,000	
Non-member	❑NT$19,000	❑NT$22,500	❑NT$3,300	❑NT$4,000	❑NT$3,300	❑NT$4,000	
IEEE student member*[3]	❑NT$8,500	❑NT$10,000	❑NT$1,350	❑NT$1,650	❑NT$1,350	❑NT$1,650	
Student non-member*[3]	❑NT$10,500	❑NT$13,000	❑NT$1,650	❑NT$2,000	❑NT$1,650	❑NT$2,000	
Extra pages fees*[2]	❑NT$2,700 each X ____ extra page(s) (at most 2 pages)						
Extra social event tickets*[3]	❑NT$2,000 each X ____ ticket(s)						
						Total	

*[1] The exchange rate is approx. NT$33 to US$1.
*[2] Extra pages fee for each paper exceeding page limit must be paid by August 10.
*[3] Student fees do not include the social event (the tour and the banquet).

Payment method:

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I will remit / have remitted the fee on _____ (Date) under the name of _____ (Name of remitter) to:

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Card No.: ☐☐☐☐ ☐☐☐☐ ☐☐☐☐ ☐☐☐☐ Expiry Date: _____/_____ (mm/yy)
CVC2 /CVV2 No.: ☐☐☐ (The last 3 digits on the reverse side of your card.)

Name of cardholder (Please print): _____

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(TAICHUNG)

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Tel No : 886 4 2324 2277
Fax No : 886 4 2324 2233
E-mail : elhtcg@evergreen-hotels.com

(ATS 09) ACCOMMODATION BOOKING FORM

The **Evergreen Laurel Hotel Taichung**, is offering special rates to attendees of the **ATS 09** in Taichung. Please complete this form, and return one copy via fax or e-mail by **23, OCT. 2009.** (Reservation made after this date would be subject to rooms availability) And fax this form as following:

(A) ROOM TYPE & SPECIAL ROOM RATE (NTD)

Room Type	Room Square	Bed Size (cm)	Fee	Special Rate (Standard Floor)	
			TWD	Single Occupied	Double occupied
Superior Room (US)	29.4 m^2	180*200	$6,400	$ 3,200	$ 3,500
Standard Twin Room (ST)	29.4 m^2	110x200*2	$6,400	$ 3,200	$ 3,500

Note :1) Per room per night 5% government tax & 10% service charge of the original rate are included.
2) A surcharge of TWD 380 will be applied for extra one daily breakfast.
3) Free for internet speedway service.
4) Complimentary fruit basket on the day of arrival.
5) Enjoy unlimited use of the health club, sauna, swimming pool and exercise facilities.

(B) RESERVATION INFORMATION (Please type or print clearly)

Guest Name: _____

Check In date:_____ Check Out date: _____

Institution: _____

Telephone: _____Fax: _____

Number of room required:

☐ Single (one king bed) ☐ Twin (two single beds) ☐ Double (one king bed)

☐ Non-smoking room (subject to room availability)

(C) TRANSPORTATION SERVICE

☐ Transport to CKS International Airport, one way charge $3,500 NT per each car. (VOVAL)

Arrival Date: _____ Flight No: _____

Departure Date: _____ Flight No: _____

(D) PAYMENT

☐ **By Credit Card:** ☐ Visa ☐ Master card ☐ American Express ☐ Diners

Card No:_____ Date of expire: _____

Signature: _____ Date:_____

(E) CONFIRMATION

The reconfirm form will be faxed back to you within 3 days by hotel reservation center.
Resv. No.# _____ Recfm. Stamp: _____

六個月內兩寸半身彩色近照兩張
Please attach two 2"x2" head & shoulder photos in color (taken within the last six months)
本表格係免費供應
This form is given FREE OF CHARGE

核發機關填註 FOR OFFICIAL USE ONLY

☐核 准 ☐拒 件

簽證類別：☐停留 ☐居留 ☐外交 ☐禮遇

入境次數：☐單次 ☐多次

簽證效期 | 停留期限 | 簽證號碼 | 簽證日期 | **費 額**

審核意見及備註：

複審官員簽章 _____

初審官員簽章 _____

中華民國簽證申請表 VISA APPLICATION FORM FOR ENTRY INTO TAIWAN, REPUBLIC OF CHINA

本表格須由申請人親自簽署,未成年兒童之申請表須由其父母或合法監護人簽署
The applicant must sign this form. Applicants who have not reached the age of majority must have the form signed by a parent or legal guardian.
請以正楷填寫各欄 Please complete all sections in **BLOCK LETTERS**

擬申請何種簽證 WHICH CATEGORY OF VISA ARE YOU APPLYING FOR ?

1.種 類： ☐停留簽證 ☐居留簽證 ☐外交簽證 ☐禮遇簽證
Category Visitor visa Resident visa Diplomatic visa Courtesy visa

2.入境次數： ☐單 次 ☐多 次
Entry Single Multiple

申請人資料 APPLICANT'S DETAILS：

姓 Surname

3.全 名(與護照所載相同)：Fullname (exactly as in passport)

名 Given name(s)

4.舊有或其他姓名 (如有)： Former or other name (if any)	5.中文姓名(如有)： Chinese name (if any)
6.國 籍： Nationality	7.舊有或其他國籍(如有)： Former or other nationality (if any)
8.性 別：☐男 ☐女 Sex Male Female	9.婚姻狀況： ☐未婚 ☐已婚 ☐鰥寡 ☐分居 ☐離婚 Marital status Single Married Widowed Separated Divorced
10.出生日期: 年Year 月Month 日Day Date of birth	11.出生地點： 市 (City) 國(Country) Place of birth _____ _____
12.職 業： Occupation	13.服務機關或就讀學校： Name of employer or school

14.在台住址及電話號碼：
Address and telephone number in Taiwan

15.本國住址及電話號碼：
Permanent address and telephone number in home country

申請人護照 APPLICANT'S PASSPORT：

16.種 類： ☐外 交 ☐公 務 ☐普 通 ☐其 他；請指明：
Type Diplomatic Official Regular Other; Please specify _____

17.號 碼： No.	**18.效期屆滿日：** 年Year 月Month 日Day **Date of expiry**
19.發照日期： 年Year 月Month 日Day Date of issue	20.發照地點： Place of issue

訪台行程 JOURNEY TO TAIWAN, R.O.C.：

21.訪台目的： ☐旅 遊 ☐洽 商 ☐就 學 ☐應 聘 ☐依（探）親 ☐宗 教
Purpose of travel Tourism Business Study Employment Joining or visiting family Religion

☐其他；(請指明)：
Other; (please specify) _____

22.預定抵台日期： 年Year 月Month 日Day Proposed date of arrival	23.預定離台日期: 年Year 月Month 日Day Proposed date of departure from Taiwan

在台關係人(如有) Particulars of Reference in Taiwan(if applicable)：

姓 名
Name _____

與申請人關係
Relationship to applicant _____

在台關係人之身分證字號或外僑居留證號碼
ROC ID / ARC No. of your reference in Taiwan.

住宅電話號碼
Telephone No. _____

住址:
Residential address _____

辦公室電話號碼
Office telephone No. _____

條碼粘貼區

★ 請據實回答以下問題 **ALL APPLICANTS ARE REQUIRED TO READ AND CHECK THE APPROPRIATE BOX FOR EACH ITEM:**

A.是否在中華民國境內或境外曾有犯罪紀錄或曾經拒絕入境、限令出境或驅逐出境？
Have you had any criminal record within or outside the territory of the R.O.C. or have you ever been denied entry, ordered to leave or deported by the R.O.C. government？…..…….. ☐YES….☐NO

B.是否曾非法入境中華民國者？
Have you ever entered Taiwan, R.O.C. illegally？……☐YES….☐NO

C.是否患有足以妨害公共衛生或社會安寧之傳染病(如愛滋病)、精神病,或吸毒或其他疾病或吸毒成癮者？
Have you ever been afflicted with a communicable disease of public health significance such as AIDS, a dangerous physical or mental disorder, or been a drug abuser or addict？……☐YES…☐NO

D.是否曾在中華民國境內逾期停留、逾期居留或非法工作？
Have you ever overstayed visitor or resident visas or worked illegally in Taiwan, R.O.C.？……...☐YES…☐NO

E.是否曾從事管制藥品(如毒品)交易？
Have you ever been a controlled substance (drug) trafficker？……..☐YES…☐NO

F.你是否曾遭中華民國駐外代表機構拒發簽證？
Have you ever been refused a visa at an R.O.C. mission？…….☐YES....☐NO

G.是否曾以其他姓名申請中華民國簽證？
Have you ever applied for an R.O.C. visa with a different name？……☐YES…☐NO

對以上任何一項的回答是「是」並非自動表示沒有資格獲得簽證。如果你的回答是「是」，或對任何一項有疑問，最好請你親自來面談。如果現在不能親自來，請另備書面說明與申請表一齊提出。

Attention : YES answer does not necessarily signify ineligibility for a visa. If you answered YES to any of the questions listed above or if you have any question in this regard, personal appearance at this office is recommended. If you are not to file the application in person, please prepare and attach a statement with explanatory notes to this form.

茲聲明 Acknowledgement :

本人確知 I certify that:

1. 已閱讀並了解申請表各節，並聲明表內所填覆之各項內容均屬確實無誤。
   I have read and understood all the questions set forth in this application and that the answers I have furnished on this form are true and correct to the best of my knowledge and belief.
2. 我明白任何虛僞或誤導的陳述都可能讓我被拒發簽證或被拒絕進入中華民國。
   I understand that any false or misleading statement may result in the refusal of a visa or denial of entry into Taiwan, the Republic of China.
3. 我同時瞭解中華民國政府有權不透露拒發簽證之原因並不予退費。
   I also understand that the government of the Republic of China reserves the right to withhold disclosure of the reasons for disapproval of my visa application, and to withhold the fees deemed non-refundable.
4. 本人所填之簽證申請表一經繳交即成爲中華民國政府所有,無法退還。
   I understand that once submitted this application form has become the property of the government of the R.O.C. and will not be returned to me.
5. 我了解在台灣曾設有戶籍的中華民國國民，一旦入境中華民國將受中華民國法律管轄。★依據役男出境處理辦法第十四條規定「在臺原有戶籍兼有雙重國籍之役男，應持中華民國護照入出境；其持外國護照入境，依法仍應徵兵處理者，應限制其出境」。另有關服兵役規定，請上內政部入出國及移民署網站：
   www.immigration.gov.tw.

I am aware that R.O.C.citizens ever registered with household in Taiwan shall be subject to the laws of the Republic of China while in its jurisdiction. According to the Regulations for Exit of Draftees Article 14：For a draftee having maintained his household registation in Taiwan and has at the same time the status of double nationalities shall enter into and depart from Taiwan by presenting his ROC passport; any draftee entering into Taiwan by presenting a foreign passport and is duly subject to conscription shall be restricted from departing from Taiwan.
For conscription law please visit the web site : www.immigration.gov.tw.

警告 WARNING :

依據中華民國刑法，販賣、運送毒品者可判處死刑。

Drug trafficking is punishable by death according to the criminal law of the Republic of China.

申請年月日 DATE OF APPLICATION : _____

申請人簽名 APPLICANT'S SIGNATURE : _____
(請親簽)　(Personal signature is required)

代理人簽名 SIGNATURE OF THE APPLICANT'S AGENT : _____

與申請人關係 Relationship to the applicant : _____

代理人全名、住址及電話 Agent's full name, address and telephone number

姓名 Name : _____　電話 Telephone No. : _____

住址 Address : _____

收件號：　　承辦人編號姓名：　　MV0101

大陸地區人民入出臺灣地區申請書

申請人資料	姓名		英文姓名（正楷填寫）		☐初次申請 ☐再次申請		
	原名（別名）		性別	☐男 ☐女	出生地	省（市）　縣（市）	身分證明號碼
	出生年月日	民國　年　月　日 （西元　年）	學歷	高中	統一證號（無則免填）		
	申請事由及代碼	学术科技活动(115)	現住地區	☐大陸 ☐港澳 ☐國外			
			所經第三地區	☐香港 ☐其他（　）	入出境證證別	☐單次 ☐逐次加簽許可證 ☐多次	
	現職	本職：					
		兼職：					
	經歷（含曾任職務、具有何種專業造詣等）						
	居住地址		電話				
	連絡地址		電話				
	證照資料	☐大陸地區護照 ☐其他	號碼		發照日期及效期		何時由何地到僑居地	地點： 時間：
	外國簽證資料	國別		種類		日期		效期		停留期限	

申請人親屬狀況	稱謂	姓名	出生年月日	存歿	職業	現住地址	電話
	父						
	母						
	配偶						
	子女						
	子女						

來臺地址（旅館）		電子郵件信箱	

探親探病奔喪對象資料	稱謂	姓名	出生年月日	身分證號	現住地址	電話及手機號碼
代申請人資料						

一、照片請貼同式最近三個月內二寸半身正面脫帽白色背景照片一張

貼照片處

二、照片背面請書寫姓名、出生日期。

代辦旅行社

註冊編號

公司及負責人戳記

本局局本部：臺北市廣州街 15 號　電話：(02)23899983
臺中服務處：臺中市南屯區干城街 91 號 1 樓　電話：(04)22549981
高雄服務處：高雄市成功一路 436 號 1 樓　電話：(07)2823740
花蓮服務處：花蓮市中山路 371 號 7 樓　電話：(038)338029
金門服務站：金門縣金城鎮賢城路 3 號莒光山莊　電話：(082)323701
馬祖服務站：馬祖南竿鄉福澳村 135 號福澳港候船大樓二樓　電話：(0836)23736

條碼編號請勿污損

申報事項	一、依臺灣地區與大陸地區人民關係條例第七十七條規定：「大陸地區人民在臺灣地區以外之地區，犯內亂罪、外患罪，經許可進入臺灣地區，而於申請時據實申報者，免予追訴、處罰。」 二、申請人現任或曾任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者，請於本欄據實詳述。如未據實填寫，經查獲或遭人檢舉者，應負法律責任。 ■申請人未曾任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者。 □申請人曾任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者，曾任職於＿＿＿＿＿＿＿＿ □申請人現任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者，現任職於＿＿＿＿＿＿＿＿

接待單位	ISCAS 2009 大會秘書處	地 址	235 台北縣中和市建八路 2 號 6 樓之 9		
		電 話	02-82261010	負責人	勞俊湘

注意事項	一、本申請書由申請人或代申請人親自據實填寫，如未據實填寫經查獲者，得撤銷其入境許可，並限期離境。由在台親屬委託他人代為送件時，應檢附委託書。 二、申請人來台期間應遵守中華民國法令，並依限離臺，且不得從事與許可目的不符之活動。

大陸地區
居民身分證影本資料

以上所填內容，俱屬事實，如有捏造或虛假情事，願負法律責任。

申請人：　　簽章　　代申請人　　簽章

核轉單位簽註同意與否意見及簽章	入出境管理局處理意見

備註	中央目的事業主管機關核准大陸地區專業人士來臺文號 機關名稱： 文號：　年　月　日　號函

申請事由（代碼）

社會交流
探親(03)
奔喪(35)
團聚(53)
探病(64)
運回遺骸骨灰(76)
探親(77)
進行刑事訴訟(78)
兩岸會談或專案活動(81)
隨行駐華(87)
飛航任務(88)
專案許可(95)
公法給付(105)
隨行團聚(133)
大陸船員(135)

文教交流
宗教活動(09)
文教活動(79)
傳習民族技藝(81)
大眾傳播活動(83)
衛生活動(91)
環保活動(94)
法律活動(99)
體育活動(102)
地政活動(112)
營建活動(113)
公共工程活動(114)
學術科技活動(115)
學術科技研究活動(116)
消防活動(119)
社會福利活動(129)

經濟交流
商務活動(金，馬)(16)
產業交流活動(82)
經貿活動(89)
交通事務活動(90)
農業活動(92)
財金活動(93)
勞工交流活動(106)
產業科技活動(117)
產業科技研究活動(118)
履行契約(126)
跨國企業內部人員調動(127)
消費者保護活動(130)
國際性會議(136)

商務活動
商務訪問(139)
商務考察(140)
商務會議(141)
演講(142)
商務研習、受訓(143)
履約服務活動(144)
參加商展(145)
參觀商展 (146)

收件號：　　承辦人編號姓名：　　MV0101

大陸地區人民入出臺灣地區申請書

申請人資料	姓名	吳XX	英文姓名（正楷填寫）	WU JIA LI	☑初次申請 ☐再次申請	
	原名（別名）	吳XX	性別	☑男 ☐女	出生地	福建省（市） 晋江(市) 縣
	出生年月日	民國 51 年 9 月 21 日（西元 1962 年）	學歷	高中	身分證明號碼	XXXXXXXXXXXXXXX
			現住地區	☑大陸 ☐港澳 ☐國外	統一證號（無則免填）	
	申請事由及代碼	学术科技活动(115)	所經第三地區	☑香港 ☐其他（ ）	入出境證別	■單次 ☐逐次加簽許可證 ☐多次
	現職	本職：云南xx公司总经理				
		兼職：xx協會理事				
	經歷（含曾任職務、具有何種專業造詣等）	xx公司經理....				
	居住地址	XX省XX市XX路43号	電話	XX-XXXXXX		
	連絡地址	XX省XX市XX路43号	電話	13XXXXXXXXX		
	證照資料	■大陸地區護照 ☐其他	號碼	XXXXXX	發照日期及效期	2010/11/26
	何時由何地到僑居地	地點： 時間：				
	外國簽證資料	國別	種類	日期	效期	停留期限

申請人親屬狀況	稱謂	姓名	出生年月日	存歿	職業	現住地址	電話
	父	吳xx		歿			
	母	蔡XX	1931.7.31	存	粮农	XX省XX市XX路43号	XXX-XXXXX
	配偶	林XX	1962.7.23	存	粮农	XX省XX市XX路43号	XXX-XXXXX
	子女	吳XX	1989.1.27	存	學生	XX省XX市XX路43号	XXX-XXXXX

來臺地址（旅館）	台北君悦大饭店			電子郵件信箱	
探親探病奔喪對象資料	稱謂	姓名	出生年月日	身分證號	現住地址	電話及手機號碼
代申請人資料						

一、照片請貼同式最近三個月內二寸半身正面脫帽白色背景照片一張。

貼照片處

二、照片背面請書寫姓名、出生日期。

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花蓮服務處：花蓮市中山路 371 號 7 樓　電話：(038)338029
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馬祖服務站：馬祖南竿鄉福澳村 135 號福澳港候船大樓二樓　電話：(0836)23736

條碼編號請勿污損

裝　訂　線　　文併　共計　人

申報事項	一、依臺灣地區與大陸地區人民關係條例第七十七條規定：「大陸地區人民在臺灣地區以外之地區，犯內亂罪、外患罪，經許可進入臺灣地區，而於申請時據實申報者，免予追訴、處罰。」 二、申請人現任或曾任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者，請於本欄據實詳述。如未據實填寫，經查獲或遭人檢舉者，應負法律責任。 ■申請人未曾任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者。 □申請人曾任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者，曾任職於＿＿＿＿＿＿＿＿ □申請人現任大陸地區黨務、行政、軍事或具政治性機關（構）、團體之職務或為其成員者，現任職於＿＿＿＿＿＿＿＿				
接待單位	ISCAS 2009 大會秘書處	地 址	235 台北縣中和市建八路 2 號 6 樓之 9		
		電 話	02-82261010	負責人	勞俊湘
注意事項	一、本申請書由申請人或代申請人親自據實填寫，如未據實填寫經查獲者，得撤銷其入境許可，並限期離境。由在台親屬委託他人代為送件時，應檢附委託書。 二、申請人來台期間應遵守中華民國法令，並依限離臺，且不得從事與許可目的不符之活動。				

大陸地區
居民身分證影本資料

以上所填內容，俱屬事實，如有捏造或虛假情事，願負法律責任。

申請人：　吳 XX　簽章　代申請人　　簽章

核轉單位簽註同意與否意見及簽章	入出境管理局處理意見
備註　中央目的事業主管機關核准大陸地區專業人士來臺文號 機關名稱： 文號：　年　月　日　號函	

申請事由（代碼）

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