ATS'08

The Seventeenth Asian Test Symposium
November 24-27, 2008, Keio Plaza Hotel Sapporo, Sapporo, JAPAN

Message to attendants of ATS 2008 from local arrangement chairs.

General Information

SPONSORS

- IEEE Computer Society, Test Technology Technical Council
- The IEICE Information and Systems Society, Technical Committee on DC
- Kyushu Institute of Technology

SUPPORTERS

SCOPE

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind. The official language of the symposium is English.

Topics of interest include, but are not limited to:

- Automatic Test Generation / Fault Simulation
- Design for Testability / Synthesis for Testability
- Built-In Self-Test / Test Data Compression
- Delay Testing
- Defect-Based Testing / IDDX Testing
- Power Issues in Test
- Fault Modeling & Diagnosis
- Memory Test / FPGA Test
- Analog and Mixed-Signal Test
- RF Testing / High-Speed I/O Test
- System-on-a-Chip Test
- Board and System Test
- Network Protocol Testing
- Design Verification and Validation
- On-Line Test
- Fault Tolerance / Dependable System
- Software Testing / Software Design for Testing
- Economics of Test

KEY DATES

ATS'08)

Ealry Registration: **Oct. 24th, 2008.**

MORE INFORMATION

For general information
General Co-Chairs: Yasuo Sato and Seiji Kajihara
(ats08-gc@dsgn.im.hiroshima-cu.ac.jp)

For submission related information
Program Chair: Kazumi Hatayama
(ats08-pc@dsgn.im.hiroshima-cu.ac.jp)

For industry session information
Industry Chair: Toshinobu Ono
(ats08-ic@dsgn.im.hiroshima-cu.ac.jp)

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Sapporo has already become winter from autumn season since Nov.4. Now, it is snow and cold in Sapporo. The maximum temperature will be 5 centigrade and the minimum one will be -2 centigrade in your stay.

When you walk along the outside of a building, the followings are required: a coat, a muffler, a glove and an umbrella. Boots may not be necessary, but shoes with a thick bottom are suitable for walking around in Sapporo. You can buy them in the Chitose airport and in department stores inside the Sapporo station. Please visit to the following web page introducing Climate and Clothes in Sapporo.

On the other hand, it is comfortable in the ATS08 conference site, Keio Plaza Hotel Sapporo, since good air conditioners work. You will be able to spend with a thin sweater inside the hotel. If you wear thick dress in the conference site, you will feel that it is very hot. We recommend you to bring a thin sweater for spending in the conference site.

We hope to see you in Sapporo, soon.

H. Yotsuyanagi and M. Hashizume, Local Arrangement Chairs

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HAMAMATSU
Mentor Graphics
RENESAS
SYNOPSYS
VERIGY

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Registration

Early Registration (until Oct. 24th, 2008)

Please fill out a registration form and E-MAIL or FAX or Mail to ATS'08 Registration Chair by October 24th.

Prof. Toshinori Hosokawa (ATS'08 Registration Chair)
E-mail: t7hosoka@cit.nihon-u.ac.jp
Fax: +81-47-474-2669
Mail Address: Dept. of Mathematical Information Eng.,
College of Industrial Technology, Nihon University,
1-2-1, Izumicho, Narashino, Chiba 275-8575, Japan

To download Registration Forms, click here for PDF, and here for Word.

Important Note:

- At least one author must register with the paper reference number by August 11.
- No registration form will be accepted after November 14. After November 14, please register at the symposium. Only the cash in Japanese Yen will be acceptable at the on-site registration desk.
- Participant lists including name, affiliation, and country will be distributed to attendees.
- REFUND POLICY: All refund requests must be in writing and received by 24 October 2008 will be reimbursed minus a 5,000 yen administrative fee. No refunds will be issued after 24 October.

Registration Fees:

Registration fees (Japanese Yen)	Symposium		Tutorial			
			Tutorial1 **AND** Tutorial2		Tutorial1 **OR** Turorial2	
	Until Oct. 24	After Oct. 24	Until Oct. 24	After Oct. 24	Until Oct. 24	After Oct. 24
IEEE member *1, 3	45,000	54,000	26,000	33,000	16,000	20,000
Non-member *3	57,000	69,000	36,000	45,000	21,000	27,000
IEEE student member *1, 3	11,000	13,000	16,000	20,000	16,000	20,000
Student non-member	14,000	17,000	16,000	20,000	16,000	20,000
Extra pages *2,4	10,000 each page(at most 2 for each regular paper)					
Extra social event tickets	10,000 each ticket					

IEEE member rate is also applied for IEICE members.
Extra pages fee for each paper more than 6 pages must be paid by August 11.
Please indicate the paper reference number above.
Registration fee for IEEE member and Non-member includes social event tickets.

Student fees do not include the social event (the reception, the tour and the banquet).
Only regular papers can apply for extra pages.

Payment Methods:

- **Bank transfer**
  （日本国内からはこちらをお選び下さい.振込手数料はご本人で負担願います．）
  Bank Name: The Bank of Tokyo-Mitsubishi UFJ Branch name: Tama Center Branch
  Account Number: 2217251
  Account Name: ATS Finance kaikei Miura Yukiya
  - Any handling fees for the bank transfer would be borne by you.
- **Credit card(VISA or MASTER)** Overseas Only.
  Sending the card number by FAX or MAIL is strongly recommended.

The Seventeenth Asian Test Symposium

http://ats08.info.hiroshima-cu.ac.jp/
Keio Plaza Hotel Sapporo, Sapporo, JAPAN
November 24-27, 2008

Registration Form

E-MAIL or FAX or Mail this form to: Toshinori Hosokawa, ATS'08 Registration Chair
E-mail: t7hosoka@cit.nihon-u.ac.jp Fax: +81-47-474-2669
Mail Address: Dept. of Mathematical Information Eng., College of IndustrialTechnology, Nihon University, 1-2-1, Izumicho, Narashino, Chiba 275-8575, Japan

Please TYPE or print BLOCK LETTERS. Fill out one form per participant. For early registration, send it back by October 24.
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Name: _____ _____ _____
(Last) (First) (Middle)

Affiliation/company: _____

Mailing address: _____

_____ _____ Tel: _____ Fax: _____ E-mail: _____
(Zip/Postal code) (Country)

IEEE membership number: _____ Paper reference number (only for authors): _____ _____ _____
IEICE membership number: _____

Registration fees (Japanese Yen)	Symposium		Tutorial				Subtotal
			Tutorial 1 and Tutorial 2		❑Tutorial1 or ❑Turorial2		
	Until Oct. 24	After Oct. 24	Until Oct. 24	After Oct. 24	Until Oct. 24	After Oct. 24	
IEEE member*1, *3	❑ 45,000	❑ 54,000	❑ 26,000	❑ 33,000	❑ 16,000	❑ 20,000	
Non-member*3	❑ 57,000	❑ 69,000	❑ 36,000	❑ 45,000	❑ 21,000	❑ 27,000	
IEEE student member*1, *3	❑ 11,000	❑ 13,000	❑ 16,000	❑ 20,000	❑ 16,000	❑ 20,000	
Student non-member*3	❑ 14,000	❑ 17,000	❑ 16,000	❑ 20,000	❑ 16,000	❑ 20,000	
Extra pages fees*2,*4	❑10,000 each X ____ extra page(s) (at most 2 for each regular paper)						
Extra social event tickets	❑10,000 each X ____ ticket(s)						
Total							

*1 IEEE member rate is also applied for IEICE members.
*2 Extra pages fee for each paper more than 6 pages must be paid by August 11. Please indicate the paper reference number above.
*3 Registration fee for IEEE member and Non-member includes social event tickets. Student fees do not include the social event (the reception, the tour and the banquet).
*4 Only regular papers can apply for extra pages.

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❑ Bank transfer (Any handling fees for the bank transfer would be borne by you.)
I will remit / have remitted the fee on _____ under the name of _____ to:
(Date) (Name of remitter)
Bank Name: The Bank of Tokyo-Mitsubishi UFJ **Branch name**: Tama Center Branch
Account Number: 2217251
Account Name: ATS Finance kaikei Miura Yukiya
(銀行：三菱東京UFJ銀行 支店：多摩センター 口座：（普通）2217251 名義：ATS Finance カイケイ ミウラユキヤ
ATMでの振り込みの場合の名義：「ATS」 または「エーテイーエス」)

❑ Credit card (Overseas only. Sending the card number by FAX or MAIL is strongly recommended.)
I pay the fee to one of the following credit cards: ❑VISA ❑MASTER CARD

Card number: _____ Expiration date: ____/____ (Month/year)

Card holder: _____
(Type or print block letters)

Signature of the card holder: _____ Date: _____

REFUND POLICY: All refund requests must be in writing and received by 24 October 2008 will be reimbursed minus a ¥5,000 administrative fee. No refunds will be issued after 24 October.

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Visa Guide

ATS'08 Organizing Committee will send visa letters (confirmation letters) to individuals requesting them. Please fill the request form and send it to Registration Chair (e-mail: ats08-rc@dsgn.im.hiroshima-cu.ac.jp) if you request visa letters.

Download the request form for visa letter

Visa letters will only be issued to:

- Speakers / Presenters,
- Committee Members,
- Attendees who have paid their registration fee in full.

Mailing visa letters often takes two or three weeks. Please request them well in advance.

Basic information about visa application can be found on the web site of The Ministry of Foreign Affairs of Japan: http://www.mofa.go.jp/j_info/visit/visa/index.html.

Please contact the diplomatic mission nearest you if you need the details about your visa application.

- For Chinese attendees, detailed information is provided on the web site of Embassy of Japan in China.

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ATS'08 at a glance

11/24 (Mon.)	9:00-12:00	Tutorial 1		
	13:30-16:30	Tutorial 2		
	18:00-20:00	Welcome Reception		
11/25 (Tue.)	9:00-10:15	Plenary Session 1		
	10:15-10:45	Coffee Break		
	10:45-12:00	Plenary Session 2		
	12:00-13:30	Lunch Time		
	13:30-14:45	3A: Test Data & Response Compression	3B: Test Generation and Fault Simulation	3C: RF Testing
	14:45-15:15	Coffee Break		
	15:15-16:30	4A: Test Compression and BIST	4B: Test Generation for Physical Faults	4C: Analog and Mixed-Signal Test
	17:00-20:30	Social Event (Sapporo Beer Garden)		
11/26 (Wed.)	9:00-10:15	5A: Delay Testing	5B: Analog Production Test 1	5C: Hybrid Method for Test Data Compression
	10:15-10:45	Coffee Break		
	10:45-12:00	6A: Fault Diagnosis	6B: Analog Production Test 2	6C: Defect Based Testing
	12:00-13:30	Lunch Time		
	13:30-14:45	7A: Panel Session	7B: Power Aware Test Generation	7C: Design for Efficient Test
	14:45-15:15	Coffee Break		
	15:15-17:00	8A: Industry Session	8B: SoC Test	8C: Design Verification and Validation
	17:00-17:45	Poster Session (Foyer)		
	18:00-20:00	Banquet		
11/27 (Thu.)	9:00-10:15	9A: Power Aware Scan Test	9B: Memory Self Test	9C: On-Line Test
	10:15-10:45	Coffee Break		
	10:45-12:00	10A: Power Aware Delay Testing	10B: Advanced Memory Test	10C: Fault Tolerance and Dependable System

WRTLT'08

ATS'08

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Advance Program

Jump to 24th, 25th, 26th, 27th

Nov 24th, 2008

9:00-12:00 Tutorial 1
Statistical Screening Methods Targeting "Zero Defect" IC Quality and Reliability

13:30- 16:30 Tutorial 2
Delay Testing: Theory and Practice

Nov 25th, 2008

9:00-10:10 Plenary Session 1

9:00-9:20 Opening Remarks

9:20-9:45 Keynote Speech 1
The Value of Extending Test Solutions
Brian STEVENS (National Semiconductor - USA)

9:45-10:10 Keynote Speech 2
Architectural Evolution and Test Requirements in Digital-Convergence Era
Kunio UCHIYAMA (Hitachi - Japan)

10:40-12:00 Plenary Session 2

10:40-11:20 Invited Talk 1
The role of DFT in Yield
Brady BENWARE (Mentor Graphics - USA)

11:20-12:00 Invited Talk 2
Issues and new Scenario for Deep sub-micron LSI design and Testing
Kunihiro ASADA (Univ. of Tokyo - Japan)

13:00-14:15 Session 3A: Test Data & Response Compression

Not All Xs are Bad for Scan Compression
Anshuman CHANDRA, Rohit KAPUR (Synopsys - USA)

Evaluation of Entropy Driven Compression Bounds on Industrial Designs

Srinivasuiu ALAMPALLY (TI - India), Jais ABRAHAM (AMD - India), Rubin A. PAREKHJI (TI - India), Rohit KAPUR, T. W. WILLIAMS (Synopsys - USA)

13:00-14:15 Session 3B: Test Generation and Fault Simulation

Untestable Fault Identification in Sequential Circuits Using Model-Checking
Jaan RAIK (Tallinn Univ. of Tech. - Estonia), Hideo FUJIWARA (NAIST - Japan), Raimund UBAR, Anna KRIVENKO (Tallinn Univ. of Tech. - Estonia)

A Test Generation Method for State-Observable FSMs to Increase Defect Coverage under the Test Length Constraint
Ryoichi INOUE, Toshinori HOSOKAWA (Nihon Univ. - Japan), Hideo FUJIWARA (NAIST - Japan)

LIFTING: a Flexible Open-Source Fault Simulator
Alberto BOSIO, Giorgio DI NATALE (LIRMM - France)

13:00-14:15 Session 3C: RF Testing

Digitally-Assisted Analog/RF Testing for Mixed-Signal SoCs
Hsiu-Ming CHANG (UCSB - USA), Min-Sheng LIN (Broadcom - USA), Kwang-Ting CHENG (UCSB - USA)

Low-Cost One-Port Approach for Testing Integrated RF Substrates
Abhilash GOYAL, Madhavan SWAMINATHAN (Georgia Tech. - USA)

Efficient Low-Cost Testing of Wireless OFDM Polar Transceiver Systems
Deuk LEE, Vishwanath NATARAJAN, R. SENGUTTUVAN, Abhijit CHATTERJEE (Georgia Tech. - USA)

15:15-16:30 Session 4A: Test Compression and BIST

Interconnect-Driven Layout-Aware Multiple Scan Tree Synthesis for Test Time, Data Compression and Routing Optimization
Katherine Shu-Min L, Jr-Yang HUANG (National Sun Yat-Sen Univ. - Taiwan)

Sequential Circuit BIST Synthesis using Spectrum and Noise from ATPG Patterns
Nitin YOGI, Vishwani D. AGRAWAL (Auburn Univ. - USA)

A Novel BIST Scheme Using Test Vectors Applied by Circuit-under-Test Itself
Jishun KUANG, Xiong OUYANG, Zhiqiang YOU (Hunan Univ. - China)

15:15-16:30 Session 4B: Test Generation for Physical Faults

XPDF-ATPG: An Efficient Test Pattern Generation for Crosstalk-Induced Faults
Sunghoon CHUN, Yongjoon KIM, Taejin KIM, Myung-Hoon YANG, Sungho KANG (Yonsei Univ. - Korea)

A Multi-Valued Algebra for Capacitance Induced Crosstalk Delay Faults
Arani SINHA (AMD - USA), Sandeep GUPTA, Melvin BREUER (USC - USA)

Increasing Defect Coverage by Generating Test Vectors for Stuck-open Faults
Yoshinobu HIGAMI (Ehime Univ.- Japan), Kewal K. SALUJA (Univ. of Wisconsin-Madison - USA), Hiroshi TAKAHASHI, Shin-ya KOBAYASHI, Yuzo TAKAMATSU (Ehime Univ. - Japan)

15:15-16:30 Session 4C: Analog and Mixed-Signal Test

Technique to Improve the Performance of Time-Interleaved A-D Converters with

Mismatches of Non-linearity
Koji ASAMI (Advantest - Japan), Hidetaka SUZUKI, Hiroyuki MIYAJIMA, Tetsuya TAURA, Haruo KOBAYASHI (Gunma Univ. - Japan)

A Reduced Code Linearity Test Method for Pipelined A/D Converters
Jin-Fu LIN, Te-Chieh KUNG, Soon-Jyh CHANG (National Cheng Kung Univ. - Taiwan)

Testing LCD Source Driver IC with Built-on-Scribe-Line Test Circuitry
Jui-Jer HUANG (National Taiwan Univ. - Taiwan), Chuan-Che LEE (Himax Technologies - Taiwan), Jiun Lang HUANG (National Taiwan Univ. - Taiwan)

Nov 26th, 2008

9:00-10:15 Session 5A: Delay Testing

Identifying Non-Robust Untestable RTL Paths in Circuits with Multi-Cycle Paths
Thomas Edison YU, Tomokazu YONEDA, Satoshi OHTAKE, Hideo FUJIWARA (NAIST - Japan)

High Quality Pattern Generation for Delay Defects with Functional Sensitized Paths
Ming-Ting HSIEH, Shun-Yen LU, Jing-Jia LIOU (National Tsing Hua Univ. - Taiwan), Augusli KIFLI (Faraday - Taiwan)

Refining Delay Test Methodology Using Knowledge of Asymmetric Transition Delay
Sean WU (UCSB - USA), Sreejit CHAKRAVARTY, Alexander TETELBAUM (LSI - USA), Li-Chung WANG (UCSB - USA)

9:00-10:15 Session 5B: Special Session: Analog Production Test 1

Effects of Advances in Analog, Mixed Signal and IO circuits on Test Strategies
Salem ABDENNADHER (Intel - USA)

Electrical Overstress Prevention & Test Best Practices
Leslie KHOO (National Semiconductor - Malaysia)

Low Distortion Sine Waveform Generation by an AWG
Akinori MAEDA (Verigy - Japan)

9:00-10:15 Session 5C: Hybrid Method for Test Data Compression

An Effective Hybrid Test Data Compression Method Using Scan Chain Compaction and Dictionary-based Scheme
Taejin KIM, Sunghoon CHUN, Yongjoon KIM, Myung-Hoon YANG, Sungho KANG (Yonsei Univ. - Korea)

Optimizing Test Data Volume Using Hybrid Compression
Brion KELLER, Sandeep BHATIA, Thomas BARTENSTEIN, Brian Foutz, Anis UZZAMAN (Cadence - USA)

Cost Efficient Methods to Improve Performance of Broadcast Scan
Seongmoon WANG, Wenlong WEI (NEC Labs America - USA)

10:45-12:00 Session 6A: Fault Diagnosis

Hyperactive Faults Dictionary to Increase Diagnosis Throughput
Chen LIU (Univ.of Iowa - USA), Wu-Tung CHENG, Huaxing TANG (Mentor Graphics - USA), Sudhakar M. REDDY (Univ. of Iowa - USA), Wei ZOU, Manish SHARMA (Mentor Graphics - USA)

Enhancing Transition Fault Model for Delay Defect Diagnosis
Wu-Tung CHENG, Brady BENWARE, Ruifeng GUO, Kun-Han TSAI, Takeo KOBAYASHI, Kazuyuki Maruo (Mentor Graphics - USA), Michinobu NAKAO, Yoshiaki FUKUI (Renesas - Japan), Hideyuki OTAKE (Renesas Design - Japan)

Observation Point Oriented Deterministic Diagnosis Pattern Generation (DDPG) for Chain Diagnosis
Fei WANG, Yu HU (ICT/CAS - China), Yu HUANG (Mentor Graphics - USA), Jing YE (Peking Univ. - China), Xiaowei LI (ICT/CAS - China)

10:45-12:00 Session 6B: Special Session: Analog Production Test 2

The HiZ problem of Power Management IC testing
Hagen GOLLER (Verigy - Germany)

Total Jitter Measurement for Testing HSIO Integrated SOCs
Takahiro YAMAGUCHI, Masahiro ISHIDA (Advantest Labs - Japan)

Load-Board/PCB Noise Suppression via Electromagnetic Band Gap Power Plane Patterning
Fidel MURADALI (National Semiconductor - USA), Suzanne HUH, Madhavan SWAMINATHAN (Georgia Inst. of Tech. - USA)

10:45-12:00 Session 6C: Defect Based Testing

Defect Detection Rate through IDDQ for Production Testing
Junichi HIRASE (JST - Japan)

Variation Aware Analysis of Bridging Fault Testing
Urban INGELSSON, Bashir M. AL-HASHIMI (Univ. of Southampton - UK), Peter HARROD (ARM - UK)

Prioritizing the Application of DFM Guidelines Based on the Detectability of Systematic Defects
Dongok KIM, Irith POMERANZ (Purdue Univ. - USA), M. Enamul AMYEEN., Srikanth VENKATARAMAN (Intel - USA)

13:30-14:45 Session 7A: Panel: How to Increase the Effectiveness of Yield Diagnostics – Is DFM the Answer to This?

Organizer/Moderator:
Anis Uzzaman (Cadence Design Systems, Inc. - USA)

Panelists:
Adit Singh (Auburn University - USA)
Srinivas Patil (Intel Corporation - USA)
Sreejit Chakravarty (LSI Corporation - USA)
Brady Benware (Mentor Graphics Corporation - USA)
Sumio Kuwabara (NEC Electronics Corporation - Japan)

13:30-14:45 Session 7B: Power Aware Test Generation

Targeting Leakage Constraints during ATPG
Goerschwin FEY (Univ. of Bremen - Germany), Satoshi KOMATSU (Univ. of Tokyo - Japan), Yasuo FURUKAWA (Advantest - Japan), Masahiro FUJITA (Univ. of Tokyo - Japan)

Power Management for Wafer-Level Test During Burn-In
Sudarshan BAHUKUDUMBI, Krishnendu CHAKRABARTY (Duke Univ. - USA)

Test Generation for State Retention Logic
Krishna CHAKRAVADHANULA, Vivek CHICKERMANE, Brion KELLER, Patrick GALLAGHER, Steven GREGOR (Cadence - USA)

13:30-14:45 Session 7C: Design for Efficient Test

Area and Test Cost Reduction for On-Chip Wireless Test Channels with System-Level Design Techniques
Chun-Kai HSU, Li-Ming DENQ, Mao-Yin WANG, Jing-Jia LIOU, Chih-Tsun HUANG, Cheng-Wen WU (National Tsing Hua Univ. - Taiwan)

On-Chip Test Generation Mechanism for Scan-Based Two Pattern Tests
Nan-Cheng LAI, Sying-Jyan WANG (National Chung-Hsing Univ. - Taiwan)

Level-Testability of Multi-Operand Adders
Nobutaka KITO, Naofumi TAKAGI (Nagoya Univ. - Japan)

15:15-17:00 Session 8A: Industry Session

System Level LBIST Implementation
Fei ZHUANG, Xiangfeng LI, Junbo JIA (Cisco Systems - China)

CooLBIST : An Effective Approach of Test Power Reduction for LBIST
Jun MATSUSHIMA, Yoichi MAEDA, Masahiro TAKAKURA (Renesas Technology Corp. - Japan)

Practical Challenges in Logic BIST Implementation - Case Studies
Shianling WU (SynTest Technologies, Inc. - USA), Hiroshi FURUKAWA (Kyushu Institute of Technology - Japan), Boryau SHEU, Laung-Terng WANG, Hao-Jan CHAO, Lizhen YU (SynTest Technologies, Inc. - USA), Xiaoqing WEN (Kyushu Institute of Technology - Japan), Michio MURAKAMI (SynTest Technologies, Inc. - USA)

USB2.0 Logic Built In Self Test Methodology
Kean Hong BOEY, Wai Mun NG, Kok Sing YAP (Intel Microelectronics (M) Sdn. Bhd. - Malaysia)

Shared At-Speed BIST for Parallel Test of SRAMs with Different Address Sizes
Tomonori SASAKI, Yoshiyuki NAKAMURA, Toshiharu ASAKA (NEC Electronics Corporation - Japan)

Experimental Results of Built-In JItter Measurement for Gigahertz Clock
Nai-Chen Daniel CHENG, Yu LEE, Ji-Jan CHEN (Industrial Technology Research Institute - Taiwan)

Leading Edge Technology and Test Noise
Takayuki KATAYAMA, Kou EBIHARA, Goro IMAIZUMI (Fujitsu Microelectronics Limited - Japan)

DFT Technique to Conclusively Translate Floating Nodes to High IDDQ Current in Analog Circuits
Ricky SMITH, Tony SHI (Texas Instruments - USA)

Diagnosis of Voltage Dependent Scan Chain Failure Using VBUMP Scan Debug Method
Khairul KHUSYARI, Wei Tee NG, Neal JAARSMA, Robert ABRAHAM, Peng Weng NG, Boon Hui ANG, Chin Hu ONG (Marvell Semiconductor - Malaysia)

Detectability of the Two-dimensional Detector for Time Resolved Emission Measurement
Nobuyuki HIRAI (Hamamatsu Photonics K.K. - Japan)

Protocol Aware Test Methodologies Using Today's ATE

Shawn MOLAVI, Andy EVANS, Ray CLANCY (Broadcom Corp. - USA)

15:15-16:55 Session 8B: SoC Test

Core-Level Compression Technique Selection and SOC Test Architecture Design
Anders LARSSON, Xin ZHANG, Erik LARSSON (Linköping Univ. - Sweden), Krishnendu CHAKRABARTY (Duke Univ. - USA)

Simulation-Driven Thermal-Safe Test Time Minimization for System-on-Chip
Zhiyuan HE, Zebo PENG, Petru ELES (Linköping Univ. - Sweden)

A Design-for-Debug (DfD) for NoC-based SoC Debugging via NoC
Hyunbean YI (Univ. of Massachusetts - USA), Sungju PARK (Hanyang Univ. - Korea), Sandip KUNDU (Univ. of Massachusetts - USA)

Accelerated Functional Testing of Digital Microfluidic Biochips
Debasis MITRA (Indian Statistical Inst. - India), Sarmishtha GHOSHAL, Hafizur RAHAMAN (Bengal Engg. and Science Univ. - India), Bhargab B. BHATTACHARYA, D. Dutta MAJUMDER (Indian Statistical Inst. - Japan), Krishnendu CHAKRABARTY (Duke Univ. - USA)

15:15-16:55 Session 8C: Design Verification and Validation

On Reusing Test Access Mechanisms for Debug Data Transfer in SoC Post-Silicon Validation
Xiao LIU, Qiang XU (Chinese Univ. of Hong Kong - Hong Kong)

A Robust Automated Scan Pattern Mismatch Debugger
Kun-Han TSAI, Ruifeng GUO, Wu-Tung CHENG (Mentor Graphics - USA)

An Interactive Verification and Debugging Environment by Concrete/Symbolic Simulations for System-level Designs
Yoshihisa KOJIMA, Tasuku NISHIHARA, Takeshi MATSUMOTO, Masahiro FUJITA (Univ. of Tokyo - Japan)

Coverage Directed Test Generation: Godson Experience
HaiHua SHEN, Wenli WEI, Yunji CHEN, Bowen CHEN and Qi GUO (ICT/CAS - China)

Nov 27th, 2008

9:00-10:15 Session 9A: Power Aware Scan Test

Test Power Reduction by Blocking Scan Cell Outputs
Xijiang LIN, Janusz RAJSKI (Mentor Graphics - USA)

Two-Gear Low-Power Scan Test
Chao-Wen TZENG, Shi-Yu HUANG (National Tsing-Hua Univ. - Taiwan)

DCScan: A Power-Aware Scan Testing Architecture
Gui DAI, Zhiqiang YOU, Jishun KUANG, Jiedi HUANG (Hunan Univ. - China)

9:00-10:15 Session 9B: Memory Self Test

Layout-Aware and Programmable Memory BIST Synthesis for Nanoscale System-on-Chip Designs
Aman KOKRADY, C.P. RAVIKUMAR (TI - India), Nitin CHANDRACHOODAN (IIT Madras - India)

A Low-Cost Pipelined BIST Scheme for Homogeneous RAMs in Multicore Chips

Yu-Jen HUANG, Jin-Fu LI (National Central Univ. - Taiwan)

A Software-Based Test Methodology for Direct-Mapped Data Cache
Yi-Cheng LIN, Yi-Ying TSAI, Kuen-Jong LEE, Cheng-Wei YEN, Chung-Ho CHEN (National Cheng Kung Univ. - Taiwan)

9:00-10:15 Session 9C: On-Line Test

Time-Multiplexed Online Checking: A Feasibility Study
Ming GAO, Hsiu-Ming CHANG, Peter LISHERNESS, Kwang-Ting CHENG (UCSB - USA)

On-Line Instruction-checking in Pipelined Microprocessors
Stefano DI CARLO (Politecnico di Torino - Italy), Giorgio DI NATALE (LIRMM - France), Riccardo MARIANI (YOGITECH - Italy)

Design of FSM with Concurrent Error Detection Based on Viterbi Decoding
Ming LI, Shiyi XU, Enjun XIA, Fayu WAN (Shanghai Univ. - China)

10:45-12:00 Session 10A: Power Aware Delay Testing

PHS-Fill: A Low Power Supply Noise Test Pattern Generation Technique for At-Speed Scan Testing in Huffman Coding Test Compression Environment
Yi-Tsung LIN, Meng-Fan WU, Jiun-Lang HUANG (National Taiwan Univ. - Taiwan)

CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme for Reducing Yield Loss Risk in At-Speed Scan Testing
Hiroshi FURUKAWA, Xiaoqing WEN, Kohei MIYASE, Yuta YAMATO, Seiji KAJIHARA (Kyushu Inst. of Tech. - Japan), Patrick GIRARD (LIRMM - France), Laung-Terng WANG (SynTest - USA), Mohammad TEHRANIPOOR (Univ. of Connecticut - USA)

Power Analysis and Reduction Techniques for Transition Fault Testing
Khushboo AGARWAL, Srinivas VOOKA, Srivaths RAVI, Rubin PAREKHJI, Arjun Singh GILL (TI - India)

10:45-12:00 Session 10B: Advanced Memory Test

Influence of Parasitic Capacitance Variations on 65nm and 32nm Predictive Model Technology SRAM Core-Cells
Stefano DI CARLO, Alessandro SAVINO, Alberto SCIONTI, Paolo PRINETTO (Politecnico di Torino - Italy)

Test and Diagnosis Algorithm Generation and Evaluation for MRAM Write Disturbance Fault
Wan-Yu LO, Ching-Yi CHEN, Chin-Lung SU, Cheng-Wen WU (National Tsing Hua Univ. - Taiwan)

GDDR5 Training – Challenges and Solutions for ATE-based Test
Hubert WERKMANN, Dong-Myong KIM (Verigy - Germany), Shinji FUJITA (Verigy - Japan)

10:45-12:00 Session 10C: Fault Tolerance and Dependable System

A Re-design Technique of Datapath Modules in Error Tolerant Applications
Doochul SHIN, Sandeep K. GUPTA (USC - USA)

Reliable Network-on-Chip Router for Crosstalk and Soft Error Tolerance
Ying ZHANG, Huawei LI, Xiaowei LI (ICT/CAS - China)

Analyses on Trend of Accidents in Financial Information Systems Reported by Newspapers from the Viewpoint of Dependability

Koichi BANDO, Kenji TANAKA (Univ. of Electro-Communications - Japan)

ATS'08

The Seventeenth Asian Test Symposium
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News: Ealry Registration closes on Oct. 24th, 2008.

Tutorials

Tutorial 1

Statistical Screening Methods Targeting "Zero Defect" IC Quality and Reliability

Presenter:
Adit Singh, Auburn University

Summary:
Integrated circuits have traditionally all been tested identically in the manufacturing flow. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize test costs by adaptively subjecting “suspect” parts to more extensive testing. The idea is similar to security screening at airports. Such methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on production circuits from IBM, Intel and LSI Logic, and NXP Semiconductor.

Tutorial 2

Delay Testing: Theory and Practice

Presenters:
Srinivas Patil, Intel Corporation
Sreejit Chakravarty, LSI Corporation

Summary:
The goal of this tutorial is to provide the background and knowledge of DFT methods, tools/methodologies and best-known industry practices necessary for implementation of delay test methodology on both custom and ASIC designs. To that end, this tutorial will cover the following key aspects of delay tests: (1) Delay test models and test application techniques, (2) Incorporating environmental conditions such as cross-talk and power droop in delay tests, (3) DFT design techniques to support scan-based delay test, (4) Relevant tools and methodologies and (5) Representative test case studies from the industry. The focus of the tutorial will be primarily scan-based delay tests with emphasis on real-world implementation using industrial case studies. On the theory front, the emphasis will be on the easy to understand theoretical concepts related to delay test, and not on the complicated algebra and theory which accompanies many theoretical works on delay test.

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Keynote Speech & Invited Talk

Keynote Speech 1 (Nov. 25th, 9:20-9:45)

The Value of Extending Test Solutions

Presenter: Brian STEVENS (National Semiconductor - USA)

Summary:
In contemporary semiconductor product creation, de-compartmentalizing and applying previously operation-specific knowledge into different functional areas is valuable. This talk presents several examples of how test engineering expertise in an analog company was levered across functional area boundaries to help solve unique technical challenges and reduce overall new product cycle time. In this direction, the audience is urged to re-examine all processes related to semiconductor product development and further the trend of extending test innovation beyond traditional definitions and applications.

Keynote Speech 2 (Nov. 25th, 9:45 - 10:10)

Architectural Evolution and Test Requirements in Digital-Convergence Era

Presenter: Kunio UCHIYAMA (Hitachi - Japan)

Summary:
For digital systems in the digital-convergence era, various functions such as communication, security, audio, video, and recognition are required in a single device. However, improving the operating frequency of an embedded LSI in the system is saturated due to the significantly increasing power consumption problem. To solve this difficulty, the architecture of an LSI has been changing greatly these few years. This talk will review the recent architecture that targets a superior performance-per-power ratio and functional flexibility and the requirements to test the newly architected SoC. As the future mainstream direction, a parallelizing architecture that places multiple CPUs and special-purpose processors on a chip and that uses a parallelizing compiler will be discussed. Reviewing the low-power circuit and device technologies that support this multi-core architecture, test requirements will also be discussed.

Invited Talk 1 (Nov. 25th, 10:40-11:20)

The role of DFT in Yield

Presenter: Brady BENWARE (Mentor Graphics - USA)

Summary:

As technology nodes continue to scale, reaching mature yields in the same time as the previous node becomes increasingly difficult. In addition, mature yields are being eroded by design sensitivities to normal process variation. To combat these challenges, chip design is being called upon more than ever to help ensure designs are manufacturable and contain sufficient capabilities to determine the root cause of failures that arise in manufacturing. This presentation will first discuss the specific challenges in Yield Analysis and Failure Analysis that are resulting in slower yield ramps and lower mature yields. Secondly, a new approach to yield enhancement which effectively incorporates DFT technologies will be presented with silicon case studies that demonstrate specifically how DFT can contribute to solving yield problems in the nm era.

Invited Talk 2 (Nov. 25th, 11:20-12:00)

Issues and new Scenario for Deep sub-micron LSI design and Testing

Presenter: Kunihiro ASADA (University of Tokyo - Japan)

Summary:
The feature size of the LSI fabrication technologies is approaching to the extreme limit of the atomic size. Devices scaled down in LSI become more attractive in speed and power consumption, but less reliable and more variable in performance parameters. The reliability problem is caused by the miniaturized size and film thickness and some of variations in device parameters are physically intrinsic, caused by such as thermo-dynamic effects. One of the most important subjects in LSI design is to find a way to maximize the potential in performance with minimizing the essential weakness in device characteristics. In testing LSI, along with the conventional problems such as increasing complexity and decreasing observability/controllability, we will be faced with new issues of long term reliability and discrepancies between testing and real applications in terms of chip environments. We may have to give up the conventional scenario of the reliable pre-screening of defect-prone LSI by testing-before-shipping. In the presentation, after reviewing issues to be faced soon in LSI design and testing, a new scenario to overcome the issues will be proposed as a possible design and testing collaboration in the extremely deep sub-micron LSI era.

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Welcom Reception

The welcome reception will be held in Keio Plaza Hotel Sapporo (Room: Rose) **from 18:00 to 20:00, Nov. 24th.**

Tour to Beer Graden & Beer Party

The tour to SAPPORO BIER GAETEN (a famous beer garden of Sapporo) and the beer party at the garden will be held **from 17:00 - 20:30, Nov. 25th.**

- 17:00 - 18:00 Tour to Beer Garden
- 18:00 - 20:00 Beer Party

Banquet

The banquet will be held at Keio Plaza Hotel Sapporo (Room: Eminence A) **from 18:00 to 20:00, Nov. 26th**.

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Accommodations

Hotel Reservation Guide at Keio Plaza Hotel Sapporo

ATS hotel reservation has been closed. Please make your reservation through Keio Plaza Hotel Web site or other travel agencies.

ACCOMMODATIONS

Reservation will be made on a first-come, first-served basis.
The room rates are valid only during the period of the symposium, i.e. **from Nov. 23 to Nov. 26**.

APPLICATIONS

Persons who wish to reserve hotel accommodations should complete the application no later than **October 24, 2008**. After October 24, hotel rooms may not be guaranteed.
Applications will be accepted via e-mail or fax.
Please indicate your order of preference in the application form.
We will send a confirmation to your e-mail. If you have not received a confirmation in one week,
please notify us by email: yanagi4@ee.tokushima-u.ac.jp

PAYMENT

Payments must be made on site by cash or by credit cards.
Bank transfer and personal check are NOT available.

CANCELLATION POLICY

The cancellation can be made by email: yanagi4@ee.tokushima-u.ac.jp until Nov. 16.
After Nov. 17, all changes and cancellations should be directed to the hotel.
Cancellation must be made **72 hours** prior to arrival.

ACCOMMODATION FEE

Room Code	Room Type	Accommodation fees *	
		Nov. 23	Nov. 24 - 26
SN	Single Room (Non-smoking)	10,500 JPY (price per person per night)	8,500 JPY (price per person per night)
SS	Single Room (Smoking)		
TN	Twin Room (Non-smoking)	19,000 JPY (price per two persons per	16,000 JPY (price per two persons per
	Twin Room		

TS	(Smoking)	night)	night)

* Tax and service charge are included

Breakfast tickets are available for 1,800 JPY each.

The website of the hotel is http://www.keioplaza-sapporo.co.jp/english/

Alternative Hotels

You can find other hotels in the neighborhood of the venue. Please visit the website http://www.welcome.city.sapporo.jp/english/staying/inn01.html.
If you want to stay one of these hotels, please reserve rooms at a hotel on your own.

ATS'08

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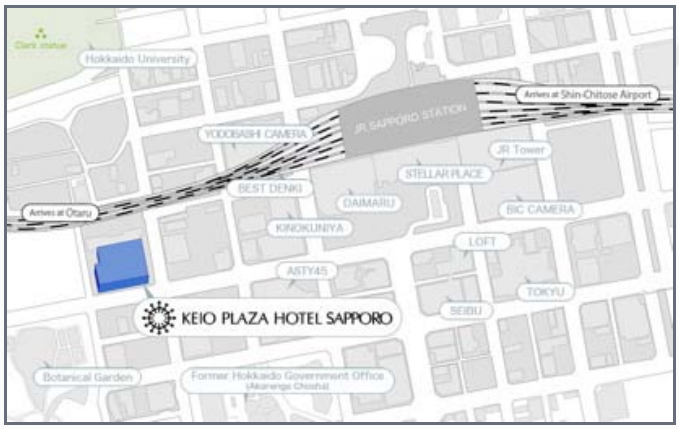
Message to attendants of ATS 2008 from local arrangement chairs.

Conference Location

The venue

Keio Plaza Hotel Sapporo
2-1 North5 West7,Chuou-ku,Sapporo,Hokkaido,Japan
tel : +81-11-271-0111fax : +81-11-271-794



*Only a 5-minute walk from JR Sapporo Statio.

Access

New Chitose Airport is the nearest airport to the Keio Plaza Hotel.
Several international and many domestic air routes are connected to the New Chitose Airport.

- International flights (map)
- Domestic flights (map)
- International/Domestic flight list

From the airport to the Keio Plaza Hotel, you can access via bus or JR train.

Access Guide and Bus Time Table (Keio Plaza Hotel)

[Bus]
70 minute bus ride from New Chitose Airport

Bus Station in New Chitose Airport Terminal
Airport Limousine Buses (platform 13 or 24)

ATS'08)

[JR train]
36 minutes by Airport Shuttle from New Chitose Airport
5 minutes walk from JR Sapporo Station

JR New Chitose Airport Station (in New Chitose Airport Terminal)

Call For Papers ATS'08

The Seventeenth Asian Test Symposium

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Sponsored by

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Kyushu Institute of Technology

SCOPE

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind. The official language of the symposium is English. Topics of interest include, but are not limited to:

- Automatic Test Generation / Fault Simulation
- Design for Testability / Synthesis for Testability
- Built-In Self-Test / Test Data Compression
- Delay Testing
- Defect-Based Testing / IDDX Testing
- Power Issues in Test
- Fault Modeling & Diagnosis
- Memory Test / FPGA Test
- Analog and Mixed-Signal Test
- RF Testing / High-Speed I/O Test
- System-on-a-Chip Test
- Board and System Test
- Network Protocol Testing
- Design Verification and Validation
- On-Line Test
- Fault Tolerance / Dependable System
- Software Testing / Software Design for Testing
- Economics of Test

SUBMISSIONS

Regular Session: The ATS'08 Program Committee invites original, unpublished paper submissions for ATS'08. Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. An abstract of 50 words or less and 5-10 keywords are also required. All submissions are to be made electronically through the ATS'08 website. Detailed instructions for submissions are to be found at the ATS'08 website. Electronic submissions in PDF files are strongly recommended.
The submission will be considered evidence that upon acceptance the author(s) will prepare the final manuscript (six pages for regular session) in time for inclusion in the proceedings and will present the paper at the Symposium.

Industry Session: This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of brief oral presentations followed by poster presentations. A one-page abstract is required for submission. Each submission should also include the complete address and designate a contact person and a presenter. Abstract submissions should be emailed to Industry Chair (ats08-ic@dsgn.im.hiroshima-cu.ac.jp).

KEY DATES (Regular Session)

Submission deadline: May 19, 2008
Notification of acceptance: July 11, 2008
Camera ready copy: August 11, 2008

KEY DATES (Industry Session)

Submission deadline: June 23, 2008
Notification of acceptance: July 11, 2008
Camera ready copy (one page): August 11, 2008

Program Committee

WWW: http://ats08.info.hiroshima-cu.ac.jp
For general information: ats08-gc@dsgn.im.hiroshima-cu.ac.jp
For submission: ats08-pc@dsgn.im.hiroshima-cu.ac.jp
For industry session: ats08-ic@dsgn.im.hiroshima-cu.ac.jp

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News: Ealry Registration closes on Oct. 24th, 2008.

Paper Submission

Paper Submission closed.

Regular Session

The ATS'08 Program Committee invites original, unpublished paper submissions for ATS'08.

- Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format.
- Authors should clearly explain the significance of the work, highlight novel features, and describe its current status.
- On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author.
- An abstract of 50 words or less and 5-10 keywords are also required.

All submissions are to be made electronically through the WelCoMe system. Detailed instructions for submissions are to be found at the website. Electronic submissions in PDF files are strongly recommended.

The submission will be considered evidence that upon acceptance the author(s) will prepare the final manuscript (six pages for regular session) in time for inclusion in the proceedings and will present the paper at the Symposium. It is also noted that the final manuscript will not be published without advance registration.

Key Dates:

Submission deadline: May 26, 2008 (Extended)
Notification of acceptance: July 11, 2008
Camera ready copy: August 11, 2008

Industrial Session

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ATS'08

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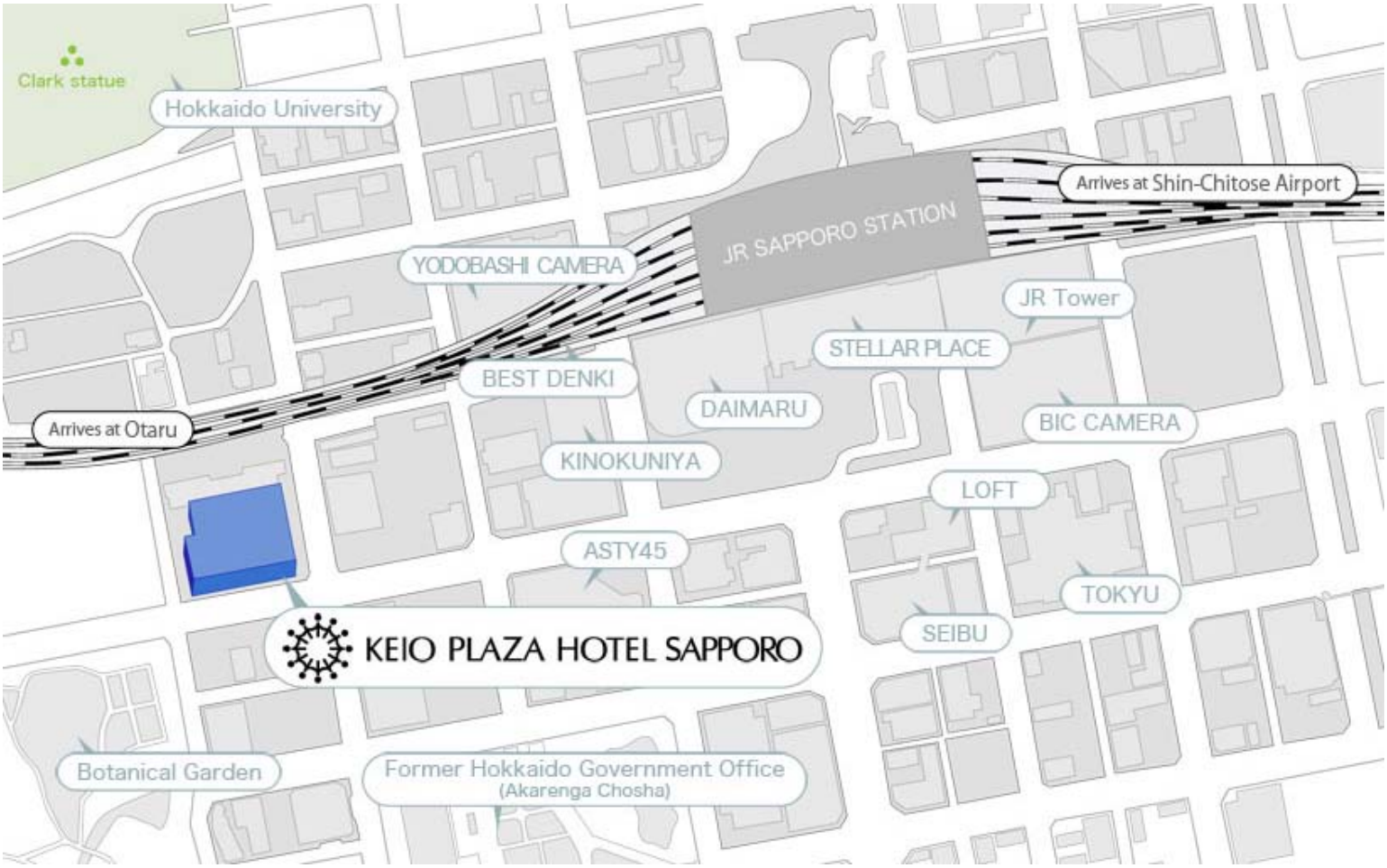
Clark statue
Hokkaido University
Arrives at Shin-Chitose Airport
JR SAPPORO STATION
YODOBASHI CAMERA
JR Tower
STELLAR PLACE
BEST DENKI
DAIMARU
BIC CAMERA
Arrives at Otaru
KINOKUNIYA
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ASTY45
TOKYU
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Botanical Garden
Former Hokkaido Government Office
(Akarenga Chosha)