Asian Test Symposium

Nov. 15-17, 2004

Caesar Park Hotel, Kenting, Taiwan

Advance Technical Program

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WELCOME REMARKS

Welcome to 2004 Asian Test Symposium (ATS'04)!

After its debut in Hiroshima, Japan in 1992, Asian Test Symposium has taken on a long journey in twelve years through cities in Asia and Pacific Region; including Hiroshima, Beijing, Nara, Bangalore, HsinChu, Akita, Singapore, Shanghai, Taipei, Kyoto, Guam, and Xi'an. This year, the symposium comes to Kenting, a national park in Taiwan. In an atmosphere full of natural beauty, we hope that new ideas about VLSI Testing can also be inspired in a more natural way.

This year, we received 122 submissions from all over the world, including 82 from Asia, 20 from America, 19 from Europe and 1 from Australia. Four reviews were solicited for each submission from 118 reviewers. The program committee meeting was held on June 29, 2004 to select 66 regular papers and 8 short papers into the final program. These papers cover nearly all aspects of the "Enabling Technology for SOC Production", including advanced DFT techniques for test cost reduction, SOC test integration, testing, diagnosis, and repair of embedded digital, analog, and memory components in an SOC.

In addition to technical sessions, ATS'04 offers one keynote speech, one invited talk, and two full-day tutorials. In the keynote speech, Dr. Bernd Koenemann offers his viewpoints of the ultimate enemy of testing in "Defects: Whose Faults Are They". In the invited talk, Prof. Melvin Breuer presents his new look at the renaissance of "Error-Tolerance and Related Test Issues". The two tutorials, in cooperation with the Test Technology Educational Program (TTEP) of the IEEE Test Technology Technical Council (TTTC), provide in-depth coverage on two hot topics: "High-Performance Test Measurements", and "Emerging Boundary Scan IEEE Std. 1149.6".

Just like previous Asian Test Symposia, we sincerely hope that you will find this event pleasant and relaxed while informative and inspiring at the same time.

Welcome to Kenting and enjoy ATS'04 !

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TTEP INFORMATION

ASIAN TEST SYMPOSIUM is sponsored by the IEEE COMPUTER SOCIETY Test Technology Technical Council (TTTC)

The Test Technology Technical council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to member's professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology.

TTTC is a prime sourced of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters and electronic broadcasts. All its activities are led by volunteer members.

TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level. To learn more about TTTC offerings and membership benefits, please visit: *http://computer.org/tttc*

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes in 2004 a comprehensive set of Test Technology Tutorials to be held in conjunction with TTTC sponsored technical meetings and included in the annual and expanding Test Technology Educational Program (TTEP). TTEP intends to serve the test and design professionals offering fundamental education and expert knowledge in state-of-the-art test technology topics.

Participation in TTEP-organized tutorials is credited by TTTC. Each full day tutorial corresponds to four TTEP units. Upon completion of each sixteen TTEP units official accreditation in the form of an "IEEE TTTC Test Technology Certificate" will be presented to the participants. In addition to the tutorials, certified university courses and industrial seminars related to test technology can also be included in TTEP and the participation in these credited similar to TTEP tutorials. For information on TTEP 2004 please visit the TTEP web site http://tab.computer.org/tttc/teg/ttep. The two full-day tutorials of the ATS 2004 technical program are part of TTEP 2004.

The Best Paper of ATS'02 at Guam

8B-1 (SoC Testing 1):
"Integrated Test Scheduling, Test Parallelization and TAM Design"
- Erik Larsson, Klas Arvidsson, Hideo Fujiwara and Zebo Peng

- Selected by Best Paper Award Committee of ATS'02

TUTORIAL A

Nov.15 9:00~12:00, 13:30~16:30
IPANEMA ROOM

Title: Signal Integrity, Jitter, and Timing Accuracy: The Basics of High Performance Test Measurements

Speaker: Thomas Warwick
Evaluation and Product Engineering, Inc.

Intended Audience:
The intended audience is the industry based test or product engineer who needs to accurately test and yield devices operating over 500Mbit/s.

Abstract:
The tutorial will explain the basis for devices errors at high speed that do not generally disturb lower speed applications. These errors will be quantified in terms of jitter and signal attenuation. Measurement techniques will be explained in some detail and the sources of measurement errors, especially relative to signal integrity, will be presented. The tutorial will conclude with a discussion of corrective methods and case studies.

Keywords:
Jitter, jitter tolerance, high speed measurement error, ISI, signal integrity, Device Interface Board, Gigabit/s test, Data Eye Measurements, Bit Error Rate

Biography: Thomas P. Warwick (Phil) graduated for Purdue University with a focus in RF micro-electronics. He has worked in the test industry most of his career for Harris Corporation and Hewlett Packard Company. Since 1995, he has been a principal consultant for EPE Inc., a training and consulting firm, specialized in serial and data communications test. Since 1998, Mr. Warwick has authored or co-authored 6 ITC papers and been voted into the "Top 10" presentation awards three times. He lives in Melbourne, FL, with his wife of 20 years, and their three daughters.

Nov.15 9:00~12:00, 13:30~16:30
PANAMA ROOM

Title: Boundary Scan Testing of Advanced Digital Networks: IEEE Std. 1149.6 Demystified

Speakers: Saghir Shaikh and Salem Abdennadher
Intel Corporation

Intended Audience:

This tutorial is suitable for design, test and DFT engineers involved in actual implementation of mixed-signal devices and systems. The CAD engineers, architects and engineering managers would also greatly benefit from this tutorial.

Abstract:

IEEE Std. 1149.6, like its predecessor IEEE Std. 1149.1, is gaining more popularity and becoming the leading test interface for all future PCB boards containing AC-coupled high-speed differential signals. Some elements of the IEEE 1149.6 architecture are similar to the IEEE 1149.1 in regards to test access port interface, TAP controller and boundary scan register, however, the implementation of the new elements, such as the input test receiver, new standard instructions, and the output test signal generation, for various technologies (i.e. LVDS, PECL, CML) is a challenging task. This tutorial illustrates the different concepts and components of IEEE 1149.6 by providing implementation examples and a description of the typical design flow for insertion and validation and suitable CAD tools. This tutorial also describes how this standard works for testing various communications systems such as Gigabit Ethernet, Transceivers and Fiber channels and others.

Keywords:

IEEE Standards 1149.6, Boundary Scan Testing, System Level

Biography: Saghir A Shaikh, BE (89), MSEE (91), and Ph.D. (96) is currently a Senior Staff Design Engineer in Wireless Networking Group of Intel Corporation. Dr. Shaikh has been a DFT architect for more than 10 mixed-signal devices and has implemented IEEE 1149.1 & IEEE 1149.6 for several devices. Dr. Shaikh has authored more than a dozen research papers in the design-for-test and computer architecture areas. These papers have been presented in various conferences such as ITC, ICCAD, VTS and other IEEE sponsored conferences. He is a member of IEEE & IEEE Computer Society.

Biography: Salem Abdennadher received the BS degree and MS degree from Oregon State University in 1990 and 1992, respectively, in Electrical and Computer Engineering. From 1992-1994, he was a research engineer at a speech synthesis and recognition research lab in Lannion, France. From 1994-1996 he was a research assistant in Motorola Austin working in digital Wireless communications. He Joined Intel in 1996 where he is working as a Staff Mixed Signal DFT Engineer. His responsibilities and interests are to ensure testability and manufacturability of Mixed Signal products. His recent publications and international patent filing in mixed signal DFT/BIST ranges from Filter BIST, on chip Jitter BIST, to Mixed signal Behavioral modeling and noise extraction and prediction. He is a member of IEEE Computer Society, IEEE Signal Processing Society, and Phi Beta Delta Honor Society for International Scholars.

KEYNOTE SPEECH

Nov.16 8:40~9:30

Title: Defects: Whose Fault Are They?

Speaker: Bernd Koenemman, Mentor Graphics Corp.

Abstract:

The experience with 130nm technologies indicates that yield loss no longer is entirely dominated by catastrophic defects due to particle contamination. Effects from sub-wavelength lithography, lower supply voltages, increasing leakage, and increasing sensitivity of parametric circuit behavior to local variations can create parametric defects and associated yield loss. Pre-signoff design closure depends on software models that attempt to predict the actual circuit behavior realized in silicon. Process design rule complexity as well as inter-chip and intra-chip variability have grown to a level where accurate predictive modeling becomes difficult. Since guard banding the models for robust design closure would lead to underutilization of technology capabilities, some increasing risk of parametric defectivity must be anticipated. Test and diagnosis have to adapt to these changing challenges.

Test generation and fault simulation tools depend on software models of circuit behavior to quantify the expected effectiveness of a test set. Where design verification tools model expected "good" circuit behavior, test and fault simulation use fault models that anticipate "defective" behavior in addition to models for "good" circuit behavior. In light of the radical changes in circuit manufacturing technologies over the past decades, it is remarkable that the fault models seem to have hardly changed since the early days of the data processing industry. The rising importance of parametric defects could challenge the validity of existing fault models and structural scan-based test methods.

Our prediction is that stuck-at faults and transition faults will survive this latest challenge like they survived many earlier challenges. However, it will become increasingly important to consider parametric conditions when generating and applying the tests. Structural scan-based tests not only have the benefit of automatic test generation, but they can also help automate and accelerate diagnosis and characterization. Hence, we predict that scan-based test methods will remain to be valuable not only for screening catastrophic defects but also for better learning of parametric "functional" circuit behavior.

Biography: Dr. Koenemann is a Fellow at Cadence Design Systems where he is responsible for defining technical and product strategies for semiconductor test, most notably a new integrated software product line that addresses the needs of debug, failure analysis, and yield management engineers, as well as some unique challenges of the dis-aggregated fabless/foundry supply chain. Dr. Koenemann came to Cadence from IBM, where, as a Distinguished Engineer, he drove the adoption of new data compression methods into the IBM's test generation software and the IBM ASIC test methodology. Prior to IBM he held other engineering, management, and executive positions at LogicVision, IBM, and Honeywell.

Dr. Koenemann is a principal inventor and early pioneer of techniques for compressing the don't-care information in automatically generated test data. This technology represents the most significant revolutionary improvement of modern commercial ATPG methods and is now in industrial use worldwide. In addition, he initiated, drove, and was a key architect of IBM's advanced scan-based delay test system, first proposed and initially helped drive the development of CTL (Core Test Language; now IEEE P1450.6), and co-invented the well-known early BILBO logic Built-In Self-Test approach.

Dr. Koenemann authored and co-authored numerous technical papers and holds several patents in the field of test technology. He has been an invited keynote speaker at ETW (European Test Workshop), and DDECS (Design&Diagnostics of Electronic Circuits&Systems), as well as an invited awards luncheon speaker at ISTFA (International Symposium on Test and Failure Analysis).

INVITED TALK

Nov.16 9:30~10:20

Title: Error-Tolerance and Related Test Issues

Speaker: Melvin Breuer, USC

Abstract:

Because of trends in scaling, in the near future every high performance dice will contain a massive number of defects and process aggravated noise and performance problems. In an attempt to obtain useful yields, designers and test engineers will need to adopt a qualitatively different approach to their work. They will need to learn, enhance and deploy techniques such as fault- and defect-tolerance. For some applications, they may even apply error-tolerance, a somewhat controversial emerging paradigm. A circuit is **error-tolerant** (ET) with respect to an application, if (1) it contains defects that cause internal and may cause external errors, and (2) the system that incorporates this circuit produces acceptable results. In this presentation we illustrate and give quantitative bounds on several factors that will shape the future of digital design. We compare and contrast defect and fault-tolerant schemes with that of error-tolerance. We discuss how yield can be optimized by appropriately selecting the granularity of spares in light of defect densities and interconnect complexity. We show that several large classes of consumer electronic applications are resilient to errors, and how error-tolerance can then be used to significantly enhance effective yield. Finally, we discuss and illustrate several test issues related to error-tolerance.

Biography: Melvin A. Breuer received his Ph.D. in electrical engineering from the University of California, Berkeley, and is the Charles Lee Powell Professor of Electrical Engineering and Computer Science at the University of Southern California. He was Chairman of the Department of Electrical Engineering-Systems from 1991-1994, and again from 2000-2003. He was Chair of the Faculty of the School of Engineering, USC, for the 1997-98 academic years. His main interests are in the area of computer-aided design of digital systems, design-for-test and built-in self-test, and VLSI circuits.

Dr. Breuer is the editor and co-author of Design Automation of Digital Systems: Theory and Techniques, Prentice-Hall; co-author of Diagnosis and Reliable Design of Digital Systems, Computer Science Press; and co-author of Digital System Testing and Testable Design, Computer Science Press 1990 and reprinted in 1995 by the

IEEE Press. He has published over 220 technical papers and was formerly the editor-in-chief of the Journal of Design Automation and Fault Tolerant Computing, on the editorial board of the Journal of Electronic Testing, and the co-editor of the Journal of Digital Systems. He was co-author of a paper that received an honorable mention award at the 1997 International Test Conference, and the co-author of the best paper at the 2000 Asian Test Symposium. He is a Life Fellow of the IEEE; was a Fulbright-Hays scholar (1972); received the 1991 Associates Award for Creativity in Research and Scholarship from the University of Southern California, the 1991 USC School of Engineering Award for Exceptional Service, the IEEE Computer Society's 1993 Taylor L. Booth Education Award, an Okawa Foundation Research (2003), and the first (2000) Engineering Faculty Council Award for Outstanding Meritorious Service to the USC School of Engineering. He was the keynote speaker at the Fourth Multimedia Technology and Applications Symposium, 1999, and the Ninth Asian Test Symposium, 2000.

Session A1: *SOC Testing*

Nov.16 10:40 – 12:00, IPANEMA ROOM

Chair: Erik Larsson, Linköping University, Sweden

A1-1 Multi-frequency Test Access Mechanism Design for Modular SOC Testing
Q. Xu, N. Nicolici, McMaster University, Canada

A1-2 Rapid and Energy-Efficient Testing for Embedded Cores
Y. Han, Y. Hu, H. Li, X. Lee, A. Chandra, Institute of Computing Technology, Chinese Academy of Sciences, China

A1-3 Constructing Transparency Paths for IP Cores Using Greedy Searching Strategy
J. Xing, H. Wang, S. Yang, Department of Automation, Tsinghua University, Beijing, China

A1-4 Adding Testability to an Asynchronous Interconnect for Globally-Asynchronous, Locally-Synchronous Systems-on-Chip
A. Efthymiou, J. Bainbridge, D. A. Edwards, University of Manchester, Greece

Session B1: *Low-Power Testing*

Nov.16 10:40 – 12:00, SAOPAULO ROOM

Chair: Chien-Mo James Li, National Taiwan University, Taiwan

B1-1 Test Power Reduction with Multiple Capture Orders
K.-J. Lee, S.-J. Hsu, C.-M. Ho, Dept. of EE, National Cheng Kung University, Taiwan

B1-2 Power-Constrained DFT Algorithms for Non-Scan BIST-able RTL Data Paths
Z. You, K. Yamaguchi, M. Inoue, J. Savir, H. Fujiwara, Nara Institute of Science and Technology, Japan

B1-3 Low Power BIST with Smoother and Scan-Chain Reorder
N.-C. Lai, Y.-H. Fu, S.-J. Wang, Institute of Computer Science, National Chung-Hsing University, Taiwan

B1-4 Techniques for Finding Xs in Test Sequences for Sequential Circuits and Applications to Test Length/Power Reduction
Y. Higami, S. Kajihara, S. Y. Kobayashi, Ehime University, Japan

Session C1: *Analog BIST*

Nov.16 10:40 – 12:00, PANAMA ROOM

Chair: Michel Renovell, LIRMM, France

C1-1 A Time Domain Built-In Self-Test Methodology for SNDR and ENOB Tests of Analog-To-Digital Converters
H.-W. Ting, B.-D. Liu, S.-J. Chang, Department of Electrical Engineering, National Cheng Kung University, Taiwan

C1-2 A New BIST Scheme Based on a Summing-Into-Timing-Signal Principle with Self Calibration for the DAC
G.-X. Chen, C.-L. Lee, J.-E. Chen, Department of Electronics Engineering, National Chiao Tung University, Taiwan

C1-3 A Sigma-Delta Modulation Based Analog BIST System with a Wide Bandwidth Fifth-Order Analog Response Extractor
H.-C. Hong, C.-W. Wu, K.-T. Cheng, Dept. of Electrical and Control Engineering, National Chiao Tung University, Taiwan

C1-4 A Built-In Loopback Test Methodology for RF Transceiver Circuits using Embedded Sensor Circuits
S. Bhattacharya, A. Chatterjee, Georgia Inst of Technology, Indian

Session A2: *Advanced DFT*

Nov.16 13:30 – 14:50, IPANEMA ROOM

Chair: Der-Chen Huang, National Chung-Hsing University, Taiwan

A2-1 Multiple Scan Tree Design with Test Vector Modification
K. Miyase, S. Kajihara, S. M. Reddy, Department of Computer Sciences and Electronics, Kyushu Institute of Technology, Japan

A2-2 An Efficient Low-Overhead Policy for Constructing Multiple Scan-Chains
J.-C. Rau, C.-H. Lin, J.-Y. Chang, Dept. of EE, Tamkang University, Taiwan

A2-3 Scan-Based BIST Using an Improved Scan forest Architecture
D. Xiang, M.-J.Chen, Y.-L. Wu, Tsinghua University, China

A2-4 The Efficient Multiple Scan Chain Architecture Reducing Test Time and Power Dissipation
I.-S. Lee, T. Ambler, Y. M. Hur, University of Texas at Austin, Korea

Session B2: *Fault Analysis*

Nov.16 13:30 – 14:50, SAOPAULO ROOM

Chair: Yoshinobu Higami, Ehime University, Japan

B2-1 Testing for Missing-Gate Faults in Reversible Circuits
J. P. Hayes, I. Polian, B. Becker, Albert-Ludwigs-University, Germany

B2-2 Properties of Maximally Dominating Faults
I. Pomeranz, S. M. Reddy, Purdue University, USA

B2-3 IDDQ Test Method Based on Wavelet Transformation for Noisy Current Measurement Environment
M. Hashizume, D. Yoneda, H. Yotsuyanagi, T. Tada, T. Koyama, I. Morita, T. Tamesada, Department of Electrical and Electronics Engineering, Faculty of Engineering, The Univ. of Tokushima, Japan

B2-4 High Level Fault Injection for Attack Simulation in Smart Cards
K. Rothbart, U. Neffe, C. Steger, R. Weiss, E. Rieger, A. Mühlberger, Graz University of Technology, Austria

Session C2: *Cross-Talk Testing*

Nov.16 13:30 – 14:50, PANAMA ROOM

Chair: Hiroshi Takahashi, Ehime University, Japan

C2-1 Efficient Identification of Crosstalk Induced Slowdown Targets
S. Nazarian, S. K. Gupta, M. A. Breuer, USC, USA

C2-2 Modeling and Testing Crosstalk Faults in Inter-Core Interconnects Including Tri-State and Bi-Directional Nets
W. Sirisaengtaksin, S. K. Gupta, USC, USA

C2-3 A New Path Delay Test Scheme Based on Path Delay Inertia
C.-L. Chen, C.-L. Lee, Department of Electronics Engineering, National Chiao Tung University, Taiwan

C2-4 A Unified Approach to Detecting Crosstalk Faults of Interconnects in Deep Sub-Micron VLSI
K. S.-M. Li, C.-L. Lee, C.-C. Su, J.-E. Chen, Department of Electronics Engineering, National Chiao Tung University, Taiwan

Session A3: *Functional Testing*
Nov.17 9:00 – 10:20, IPANEMA ROOM

Chair: Debesh K. Das, Jadavpur University, India

A3-1 Efficient Template Generation for Instruction-Based Self-Test of Processor Cores
K. Kambe, M. Inoue, H. Fujiwara, Nara Institute of Science and Technology, Japan

A3-2 Test Instruction Set (TIS) for High Level Self-Testing of CPU Cores
S. Shamshiri, H. Esmaeilzadeh, Z. Navabi, University of Tehran, Iran

A3-3 A Snapshot Method to Provide Full Visibility for Functional Debugging Using FPGA
C.-L. Chuang, D.-J. Lu, C.-N. Liu, National Central University Department of Electrical Engineering, Taiwan

A3-4 A Systematic Way of Functional Testing for VLSI Chips
S. Xu, Shanghai University, China

Session B3: *Logic BIST*
Nov.17 9:00 – 10:20, SAOPAULO ROOM

Chair: Kiyoshi Furuya,Chuo University, Japan

B3-1 Weighted Pseudo-Random BIST for N-detection of Single Stuck-At Faults
C. Yu, S. M. Reddy, I. Pomeranz, ECE Dept., University of Iowa, USA

B3-2 A BIST Approach to On-Line Monitoring of Digital VLSI Circuits
S. Biswas, S. Mukhopadhyay, A. Patra, Department of Electrical Engineering, Indian Institute of Technology, Kharagpur, Indian

B3-3 Seed Selection Procedure for LFSR-based BIST with Multiple Scan Chains and Phase Shifters
M. Arai, H. Kurokawa, K. Ichino, S. Fukumoto, K. Iwasaki, Graduate School of Engineering, Tokyo Metropolitan University, Japan

B3-4 Nonlinear CA Based Design of Test Set Generator Targeting Pseudo-Random Pattern Resistant Faults
S. Das, A. Kundu, B. K. Sikdar, CST, B. E. College, Indian

Session C3: *Fault Diagnosis*

Nov.17 9:00 – 10:20, PANAMA ROOM

Chair: Shyue-Kung Lu, Fu-Len Catholic University, Taiwan

C3-1 Compactor Independent Direct Diagnosis
W.-T. Cheng, K.-H. Tsai, Y. Huang, N. Tamarapalli, J. Rajski, Mentor Graphics Corporation, USA

C3-2 Scan Chain Fault Identification Using Weight-Based Codes for SoC Circuits
S. Ghosh, K.-W. Lai, W.-B. Jone, S.-C. Chang, University of Cincinnati, USA

C3-3 Enhancing BIST Based Single/Multiple Stuck-At Fault Diagnosis by Ambiguous Test Set
H. Takahashi, Y. Yamamoto, Y. Higami, Y. Takamatsu, Ehime University, Japan

C3-4 Failure Analysis of Open Faults by Using Detecting /Un-detecting Information on Tests
Y. Sato, H. Takahashi, Y. Higami, Y. Takamatsu, Ehime University, Japan

Session A4: *SOC Test Scheduling*

Nov.17 10:40 – 12:20, IPANEMA ROOM

Chair: Chih-Tsun Huang, National Tsing-Hua University, Taiwan

A4-1 Hybrid BIST Test Scheduling Based on Defect Probabilities
Z. He, G. Jervan, Z. Peng, Linköping University, Sweden

A4-2 Pair Balance-Based Test Scheduling for SOCs
Y. Hu, Y.-H. Han, H.-W. Li, T. Lv, X.-W. Li, Information Network Laboratory, Institute of Computing Technology, Chinese Academy of Sciences, China

A4-3 RAIN : RAndom INsertion Scheduling Algorithm for SoC Test
J. B. Im, S. Chun, G. Kim, J. H. An, S. Kang, Yonsei University, Korea

A4-4 March Based Memory Core Test Scheduling for SOC
W.-L. Wang, Department of Electronic Engineering, Cheng Shiu University, Taiwan

A4-5 An Integrated Technique for Test Vector Selection and Test Scheduling under Test Time Constraint
S. Edbom, E. Larsson, Linköping University, Sweden

Session B4: *Memory Testing*
Nov.17 10:40 – 12:20, SAOPAULO ROOM

Chair: Wu-Tung Cheng, Mentor Graphics Corporation, USA

B4-1 On Test and Diagnostics of Flash Memories
C.-T. Huang, J.-C. Yeh, Y.-Y. Shih, R.-F. Huang, C.-W. Wu, National Tsing Hua University, Taiwan

B4-2 Resistive-Open Defects in Embedded-SRAM Core Cells: Analysis and March Test Solution
L.Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan, LIRMM, Université de Montpellier II, France

B4-3 A Measurement Unit for Input Signal Analysis of SRAM Sense Amplifier
Y.-M. Sheng, M.-J. Hsiao, T.-Y. Chang, Dept. of EE, National Tsing Hua Uinv., Taiwan

B4-4 An Efficient Diagnosis Scheme for Random Access Memories
J.-F. Li, C.-D. Huang, Department of EE, National Central University, Taiwan

B4-5 Evaluation of Intra-Word Faults in Word-Oriented RAMs
S. Hamdioui, J. D. Reyes, Z. Al-Ars, Philips Semiconductor Crolles R&D, France

Session C4: *Analog Testing*
Nov.17 10:40 – 12:20, PANAMA ROOM

Chair: Christian LANDRAULT, LIRMM, France

C4-1 Low-Cost Analog Signal Generation Using A Pulse-Density Modulated Digital ATE Channel
J. Rivoir, Agilent Technologies, Germany

C4-2 A Low-Cost Diagnosis Methodology for Pipelined A/D Converters
C.-H. Huang, K.-J. Lee, S.-J. Chang, Dept. of EE, National Cheng Kung University, Taiwan

C4-3 Reconfiguration for Enhanced Alternate Test (REALTEST) of Analog Circuits
G. Srinivasan, S. Goyal, A. Chatterjee, Georgia Institute of technology, USA

C4-4 Dynamic Analog Testing via ATE Digital Test Channels
C.-C. Su, C.-S. Chang, H.-W. Huang, D.-S. Tu, C.-L. Lee, C.-H. Lin, Natsional Chiao Tung University, Taiwan

Session A5: *Testable Design*

Nov.17 13:30 – 14:50, IPANEMA ROOM

Chair: Shiyu Xu, Shanghai University, China

A5-1 Design and Implementation of Self-Testable Full Range Window Comparator

M. Wong, Y. Zhang, The Hong Kong Polytechnic University, China

A5-2 Efficient Test Methodologies for Conditional Sum Adders

J.-F. Li, C.-C. Hsu, Department of EE, National Central University, Taiwan

A5-3 A Novel Approach for On-line Testable Reversible Logic Circuit Design

D.-P. Vasudevan, P. K. Lala, and P.Parkerson, University of Arkansas, USA

A5-4 Nonlinear CA Based Scalable Design of On-Chip TPG for Multiple Cores

S. Das, B. K. Sikdar, P. P. Chaudhuri, Bengal Engineering College (DU), India

Session B5: *Testability Analysis*

Nov.17 13:30 – 14:50, SAOPAULO ROOM

Chair: Ching-Hwa Cheng, Feng-Chia University, Taiwan

B5-1 Circuit Width Based Heuristic for Boolean Reasoning

G. Li, X. Li, Institute of Computing Technology, Chinese Academy of Sciences, China

B5-2 Max-Testable Class of Sequential Circuits Having Combinational Test Generation Complexity

D. K. Das, T. Inoue, S. Chakraborty, H. Fujiwara, Jadavpur University, India

B5-3 Classification of Sequential Circuits Based on k Notation

C. Y. Ooi, H. Fujiwara, Nara Institute of Science and Technology, Japan

B5-4 Detection of Reconvergent Branch Pairs

E. Edirisuriya, S. Xu , Shanghai University, China

Session C5: *Yield and Reliability*

Nov.17 13:30 – 14:50, PANAMA ROOM

Chair: Jwu-E Chen, National Central University, Taiwan

C5-1 Burn-In Stress Test of Analog CMOS ICs
C.-L. Wey, M.-Y. Liu, National Central University, Taiwan

C5-2 Fail Pattern Identification for Memory Built-In Self-Repair
R.-F. Huang, C.-L. Su, C.-W. Wu, S.-T. Lin, K.-L. Luo, Y.-J. Chang, Department of Electrical Engineering, National Tsing Hua University, Taiwan

C5-3 Reduce Yield Loss in Delay Defect Detection in Slack Interval
H. Yan, A. D. Singh, Electrical & Computer Engineering Department, Auburn University, USA

C5-4 Considering Fault Dependency and Debugging Time Lag in Reliability Growth Modeling during Software Testing
C.-Y. Huang, C.-T. Lin, Department of Computer Science, National Tsing Hua University, Taiwan

Session A6: *Fault Tolerance*

Nov.17 15:10 – 16:30, IPANEMA ROOM

Chair: Xiaowei Li, Chinese Academy of Sciences, China

A6-1 Intelligible Test Techniques to Support Error-Tolerance
M. Breuer, University of Southern Calif., USA

A6-2 Bounding Rollback-Recovery of Large Distributed Computation in WAN Environment
J.-M. Yang, D.-F. Zhang, X.-D. Yang, Hunan University, China

A6-3 Full Restoration of Multiple Faults in WDM Networks without Wavelength Conversion
C.-C. Sue, J.-Y. Yeh, Dep. of CSIE, National Cheng Kung University, Taiwan

A6-4 On Improvement in Fault Tolerance of Hopfield Neural Networks
N. Kamiura, T. Isokawa, N. Matsui, Department of Electrical Engineering and Computer Sciences, Graduate School of Engineering, University of Hyogo, Japan

Session B6: *FPGA Testing and Test Reduction*

Nov.17 15:10 – 16:30, SAOPAULO ROOM

Chair: Terumine Hayashi, Mie University, Japan

B6-1 Multiple Fault Detection and Diagnosis Techniques for Lookup Table FPGA's
S.-K. Lu, H.-C. Wu, S.-J. Yan, Y.-C. Tsai, Department of Electronic Engineering, Fu Jen Catholic University, Taiwan

B6-2 Device Resizing Based Optimization of Analog Circuits for Reduced Test Cost: Cost Metric and Case Study
D. Han, A. Chatterjee, Georgia Institute of Technology, USA

B6-3 A Test Decompression Scheme for Variable-Length Coding
H. Ichihara, M. Ochi, M. Shintani, T. Inoue, Hiroshima City University, Japan

B6-4 Alternative Run-Length Coding through Scan Chain Reconfiguration for Joint Minimization of Test Data Volume and Power Consumption in Scan Test
Y. Shi, S. Kimura, N. Togawa, M. Yanagisawa, T. Ohtsuki, Waseda Univ., Japan

Session C6: *Delay Testing*

Nov.17 15:10 – 16:30, PANAMA ROOM

Chair: Kazumi Hatayama, Renesas Technology Corporation, Japan

C6-1 Modeling and Simulation for Crosstalk Aggravated by Weak-Bridge Defects between On-Chip Interconnects.
L. Wang, S. K. Gupta, M. A. Breuer, University of Southern California, USA

C6-2 A Post-Processing Procedure of Test Enrichment for Path Delay Faults
I. Pomeranz, S. M. Reddy, Purdue University, USA

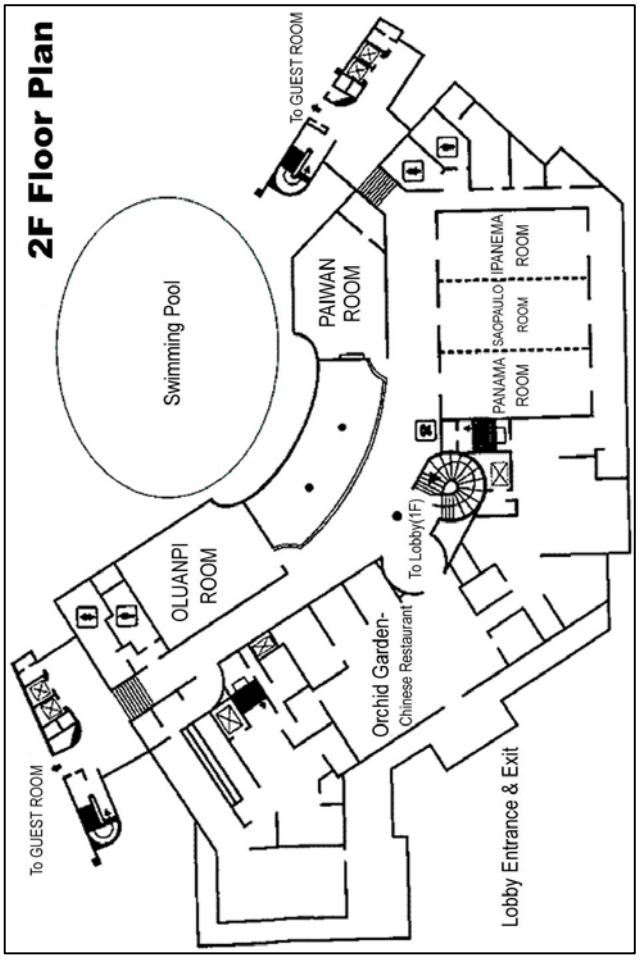
C6-3 Functional Scan Chain Design at RTL for Skewed-Load Delay Fault Testing
H.-F. Ko, N. Nicolici, McMaster University, Canada

C6-4 Analysis and Attenuation Proposal in Ground Bounce
A. Zenteno, M. Renovell, National Institute of Astrophysics, Optics and Electronics-INAOE, Europe

Hotel Floor Map

The Caesar Park Hotel-Kenting
Address: 6 Kenting Road, Hengchun Town, Pingtung, Taiwan
Tel: +886-8-886 1888
Fax: +886-8-886 1818

2F Floor Map of the Caesar Park Hotel



Program I (Outdoor):
Tour In Kenting Forest Recreation Area
Time: Nov. 16, 15:10-17:10

Buses will leave at 15:10 and take us to a relaxed and guided tour in this Kenting Forest Area, a tropical garden full of indigenous trees and plants. All sorts of dripstone caves and valleys are also interesting for you to explore.

Program II (Outdoor at the Pool Side):
Banquet with Musical Performance by Band Masaru
Time: Nov.16, 18:10-20:10

Aboriginal band Masaru will play traditional instruments and give you a musical performance with exotic flavors along with the pool-side banquet.

Program III (Indoor):
Folk Art Exhibition
Time: Nov.16, 20:10-21:10

Want to know all sorts of folk arts local people enjoy doing in their leisure time? Welcome to this exhibition and try it out yourself.

Travel Map of Kenting:

Several Travel Websites:

The Caesar Park Hotel
http://www.caesarpark.com.tw/
Kenting National Park
http://www.ktnp.gov.tw/
Kaohsiung International Airport
http://www.kia.gov.tw/
CKS International Airport
http://www.cksairport.gov.tw/
Heng-Chun Peninsula Route
http://www.tbnsa.gov.tw/

For More Information:

E-mail: ats04@larc.ee.nthu.edu.tw
WWW: http://ats04.ee.nthu.edu.tw/~ats04

ATS2004 At-A-Glance

Date	Time	Sessions		
		IPANEMA ROOM	**SAOPAULO ROOM**	**PANAMA ROOM**
Nov. 15 (Mon.)	9:00 | 12:00	Tutorial A1 (Thomas Warwick) IPANEMA ROOM		Tutorial B1 (Dr. Saghir Shaikh & Salem Abdennadher) PANAMA ROOM
	12:00 13:30	Lunch		
	13:30 | 16:30	Tutorial A2 (Thomas Warwick) IPANEMA ROOM		Tutorial B2 (Dr. Saghir Shaikh & Salem Abdennadher) PANAMA ROOM
Nov. 16 (Tue.)	8:30 | 8:40	Opening Ceremony		
	8:40 | 9:30	Keynote Speech (Dr. Bernd Koenemann)		
	9:30 | 10:20	Invited Talk (Prof. Melvin Breuer)		
	10:20 10:40	Coffee Break		
	10:40 | 12:00	**Session A1** SOC Testing	**Session B1** Low-Power Testing	**Session C1** Analog BIST
	12:00 13:30	Lunch		
	13:30 | 14:50	**Session A2** Advanced DFT	**Session B2** Fault Analysis	**Session C2** Cross-Talk Testing
	15:20 21:00	Social Program		
Nov. 17 (Wed.)	9:00 | 10:20	**Session A3** Functional Testing	**Session B3** Logic BIST	**Session C3** Fault Diagnosis
	10:20 10:40	Coffee Break		
	10:40 | 12:20	**Session A4** SOC Test Scheduling	**Session B4** Memory Testing	**Session C4** Analog Testing
	12:20 13:30	Lunch		
	13:30 | 14:50	**Session A5** Testable Design	**Session B5** Testability Analysis	**Session C5** Yield and Reliability
	14:50 15:10	Coffee Break		
	15:10 | 16:30	**Session A6** Fault Tolerance	**Session B6** FPGA Testing & Test Reduction	**Session C6** Delay Testing