Tutorials

Tutorial 1: *High Performance/Delay Testing*

Monday, Dec. 4, 8:30 am-12:00 pm and 1:30 pm-5:00 pm; R110
Presenter: S. M. Reddy, University of Iowa, USA
Chair: Shi-Yu Huang, National Tsing Hua University, Taiwan
Audience: Test engineers in semiconductor manufacturing companies, IP designers, test tool developers, graduate students, and faculty.

Description: Manufacturing defects and process variations cause a manufactured device to fail performance requirements. Defects and process variations causing these failures are detected and diagnosed by testing for delay defects. Several fault models have been proposed to capture the effect of the delay defects. These include transition faults, gate delay faults, and path delay faults. Delay defects may cause some circuit paths to exhibit larger than expected delays as well smaller than expected delays. The latter defects are called short delay defects and the former are called long delay defects.

In this tutorial we will discuss fault models, fault simulation, test generation, design for test methods and built-in-self test methods. Methods to handle the enoromous numbers of paths in large circuits called non-enumerative methods will also be discussed.

About the Presenter: Sudhakar Reddy obtained his undergraduate degree in Electrical and Communication Engineeing from Osmania Unversity, M.S. degree from Indian Institute of Science, and Ph.D. degree in Electrical Engineering from the University of Iowa, Iowa City, Iowa. Dr. Reddy has been active in the areas of testable designs and test generation for logic circuits since 1972. He has been an associate editor and twice a guest editor of IEEE Transactions on Computers. He was Program Committee Chair for 1989 International Symposium on Fault- tolerant Computing. Since 1968 he has been a member of the faculty of the Department of Electrical and Computer Engineering, University of Iowa, where he is currently the Department Chairman. In 1990 he was made a University of Iowa Foundation Distinguished Professor. In 1995 he received the Von Humboldt Senior Researcher Fellowship. He is currently an associate editor of IEEE Transcations on CAD. He is a Fellow of IEEE.

Dr. Reddy has served on the Technical Advisory Board of Sunrise Test Systems. He has been a consultant to Honeywell Inc, AT&T Bell Labs, Rockwell-Collins, and Mentor Graphics. Dr. Reddy has presented tutorials on Delay Fault Testing at International Test Conference for several years.

Tutorial 2: *SoC Testing & P1500 Standard*

Monday, Dec. 4, 8:30 am-12:00 pm and 1:30 pm-5:00 pm; R105
Presenter: Y. Zorian , LogicVision, USA
Chair: Tsin-Yuan Chang, National Tsing Hua University, Taiwan
Audience: Designers, test engineers and researchers interested in learning about the state-of-the-art in embedded test methods for complex systems-on-chip and beyond.

Description: Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. This tutorial presents the state-of-the-art in system-level integration and addresses the strategies and current industrial practices in the test of system-on-chip. It discusses the requirements for test reuse in hierarchical design, such as embedded test strategies for individual cores, test access mechanisms, test interface standardization, optimizing test resource partitioning, and embedded test management and integration at the System-on-Chip level.

About the presenter: Yervant Zorian is the Chief Technology Advisor of LogicVision Inc. Previously, he was a Distinguished Member of Technical Staff at Bell Labs, Lucent Technologies, Test and Reliability Center of Excellence. His activities include the areas of embedded core, IC and Multi-Chip Module DFT methodologies. Zorian received an MSc degree from the University of Southern California, and a PhD from McGill University. He is currently the Editor-in-Chief of IEEE Design & Test of Computers. He founded and chairs the TECS workshop; and the IEEE P1500 Embedded Core Test Standardization Working Group. He has provided tutorials and courses at numerous conferences and academic programs (such as ITC, ICCAD, DATE, VTS, ETW, etc). He was granted several patents in the domain of embedded test and received a number of Best Paper Awards. He is a Fellow of IEEE.