ATS2000 Schedule

Mon., Dec. 4

08:30 ∫ 12:00	Tutorial 1A *High Perfor-mance/ Delay Testing* S. M. Reddy R110	Tutorial 2A *SoC Testing & P1500 Standard* Y. Zorian R105
12:00 13:30	Lunch	
13:30 ∫ 17:00	Tutorial 1B *High Perfor-mance/ Delay Testing* S. M. Reddy R110	Tutorial 2B *SoC Testing & P1500 Standard* Y. Zorian R105
17:00 ∫ 18:00	Break	
18:00 ∫ 20:30	Reception	

Tue., Dec. 5

08:10 ∫ 08:30	Opening Ceremony R100	
08:30 ∫ 09:20	Keynote Speech I *Testing in the Fourth Dimension* V. D. Agrawal R100	
09:20 ∫ 10:10	Keynote Speech II *Challenges for the Academic Test Community* M. A. Breuer R100	
10:10 10:30	Coffee break	
10:30 ∫ 12:00	Industry Session *CAD Tools on Testing* R100	
12:00 13:30	Lunch	
13:30 ∫ 14:50	Taiwan Industry Session R100	
14:50 15:10	Coffee break	
15:10 ∫ 16:35	Panel Discussion I *Mixed-Signal SoC Testing* R110	Panel Discussion II *Collaboration between Industry and Academia in Test Research* R105
16:35 16:45	Short Break	
16:45 ∫ 18:00	Session A1 *Analog & Mixed Signal Test I* R110	Session A2 *Memory BIST & Self-Diagnosis* R105
18:15 ∫ 21:30	Banquet and Social Program ChiRing Hall	

Wed., Dec. 6

08:00 ∫ 09:35	Session B1 *Analog & Mixed Signal Test II* R110	Session B2 *Fault Simulation & Timing Simulation* R102	Fringe Meeting *SoC Testing & P1500 Standard* R105
09:35 09:55	Coffee break		
09:55 ∫ 11:10	Session C1 *Fault Analysis I* R110	Session C2 *Test Generation I* R102	Session C3 *Functional Testing* R105
11:10 11:20	Short break		
11:20 ∫ 12:20	Session D1 *Built-in Self-Test I* R110	Session D2 *Software Testing & Test Synthesis* R102	Session D3 *Embedded-Core Testing* R105
12:20 13:30	Lunch		
13:30 ∫ 15:05	Session E1 *Memory Testing* R110	Session E2 *Test Generation II* R102	Session E3 *IDDQ Testing* R105
15:05 15:25	Coffee break		
15:25 ∫ 16:40	Session F1 *Built-in Self-Test II* R110	Session F2 *Testability Analysis & Design for Testability* R102	Session F3 *Fault Tolerance* R105
16:40 16:50	Short Break		
16:50 ∫ 17:50	Session G1 *Fault Analysis II* R110	Session G2 *Low-Power Testing* R102	Session G3 *Self- Checking Circuits* R105

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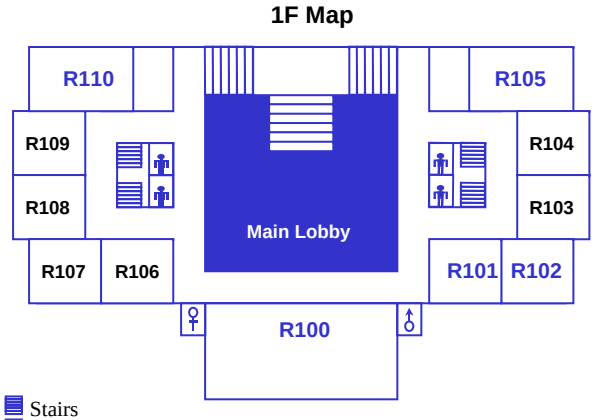
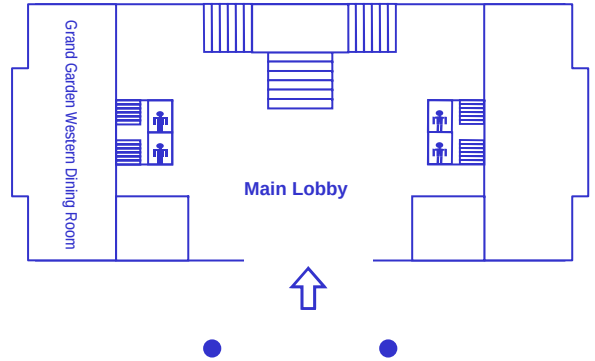
Symposium Site Map

1F Map



Stairs
Elevators
Women's Lavatory
Men's Lavatory

Lobby Map



R100: Plenary Sessions, Industry Sessions.
R101: ATS Activity Meetings.
R102: Technical Paper Session 2.
R105: Tutorial 2, Panel 2, Fringe Meeting, Technical Paper Session 3.
R110: Tutorial 1, Panel 1, Paper Session 1.

Introduction

The Asian Test Symposium (ATS), in its nine years of history, has come to Taiwan twice. Last time we met in Hsinchu, the Silicon Valley of Taiwan, in 1996. This time we will meet in Taipei, the capital city of Taiwan. If Hsinchu is the most energetic city, then Taipei is the most dynamic and colorful one in Taiwan. The two cities are playing a vital role in Taiwan's economy. If you missed Hsinchu last time, you still have a chance to visit the amazing city this time. It is only a one-hour drive from the Grand Hotel in Taipei to the Science-Based Industrial Park (SBIP) in Hsinchu. For your information, another SBIP is being established in Tainan, located in the southern part of Taiwan. As for Taipei, I need not say much. You will see for yourselves. It is a very interesting city for almost anyone.

The tradition of ATS is being maintained, with several innovations this year. We received 110 paper submissions from all over the world, including 69 from Asia, 25 from America, 15 from Europe and 1 from Australia. These papers were sent to more than 100 reviewers worldwide with 5 reviewers being solicited for each paper, and on average 4.3 reviews were returned. The Program Committee met on June 30, 2000 and made the selection of 75 papers (one withdrawn later), which were allocated into 19 paper sessions that cover most aspects of electronic testing. Starting from this year, we will have an ATS best paper competition based on the evaluations of reviewers, session chairs/attendees, and an invited panel of judges. The best paper of ATS 2000 will be presented in ATS 2001 in Japan.

In addition to the paper sessions, this year we offer two full-day tutorials, one on High Performance/Delay Testing and the other on P1500/SoC Testing. We are proud that this is the first time that the ATS offers tutorials in corporation with the Test Technology Educational Program of the IEEE Test Technology Technical Council (TTTC). In company with the tutorial on P1500/SoC Testing, we have also arranged a fringe meeting on this topic. The participants, all being test experts from industry, will discuss and share their experiences and views on P1500/SoC testing. Though being a fringe meeting, all ATS 2000 attendees are welcome to participate in the discussion.

Two special industry sessions are offered. The "CAD Tools on Testing" session is an attempt to bring together the world-recognized test tool providers to explain "Why we need test tools and what can and should be done in the future." One major purpose of this session is to draw the attention of the academia to the excellent educational promotion programs offered by most tool providers. We believe that to successfully design a reliable product will require extensive use of test tools in the near future. The "Taiwan Test Industry" session focuses on the "Value Added Testing in Taiwan." With the

strong supports from the foundry and manufacturing sectors, the design sector has seen an unsurpassed opportunity in the new Millennium. The shift in the paradigm will have a significant impact on the test sector. In this session, topics on how the test sector shall react, what the emerging technologies are, and what the new business protocol should be, will be discussed by representatives from local design, test service, and ATE companies.

The two keynotes entitled “Testing in the Fourth Dimension” and “Challenges for the Academic Test Community,” will address the challenges in testing when we enter the 21st century from the industry and the academic points of views, respectively. Some most-advanced test technologies and future research directions will be discussed, with the relationship between industry and academic research also being touched. The discussion on this relationship will continue in a panel entitled “Collaboration between academia and industry in test research,” where experienced representatives from both sides will discuss the collaboration models, possible research topics, and, more importantly, how to reach the balance that “high-risk,” basic research will not be discouraged when practical thinking is brought into the academic research. The other panel discussion concerns the fact that, while we have been enjoying the rich skills and techniques available in digital testing, we can no longer ignore the analog or mixed-signal test problems when entering the SoC and deep sub-micron era. The panel on “Mixed-Signal SoC Testing: Is Mixed-Signal Design-for-Test on Its Way?” is exactly for this purpose.

We hope that you will find the ATS 2000 program informative and thought-provoking. Though several innovations have been provided in ATS2000, one thing never changes in ATS: this is the place where we meet old friends and meet new ones. “I feel very happy when I have friends coming from afar,” said Confucius. We feel the same. The weather in early December is quite pleasant. It is a good idea to stay a few more days in Taipei or visit other parts of the island to meet more new friends.

Welcome to Taipei and enjoy ATS2000!

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Hsin-Chu, Taiwan

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Program Co-chair
Dept. of Electrical Engineering
National Cheng Kung University
Tainan, Taiwan

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Wen-Ben Jone	Sudhakar M. Reddy	Massaki Yoshida
Jing-Yang Jou	Kewal K. Saluja	Yervant Zorian

Tutorials

Tutorial 1: *High Performance/Delay Testing*

Monday, Dec. 4, 8:30 am-12:00 pm and 1:30 pm-5:00 pm; R110

Presenter: S. M. Reddy, University of Iowa, USA

Chair: Shi-Yu Huang, National Tsing Hua University, Taiwan

Audience: Test engineers in semiconductor manufacturing companies, IP designers, test tool developers, graduate students, and faculty.

Description: Manufacturing defects and process variations cause a manufactured device to fail performance requirements. Defects and process variations causing these failures are detected and diagnosed by testing for delay defects. Several fault models have been proposed to capture the effect of the delay defects. These include transition faults, gate delay faults, and path delay faults. Delay defects may cause some circuit paths to exhibit larger than expected delays as well smaller than expected delays. The latter defects are called short delay defects and the former are called long delay defects.

In this tutorial we will discuss fault models, fault simulation, test generation, design for test methods and built-in-self test methods. Methods to handle the enoromous numbers of paths in large circuits called non-enumerative methods will also be discussed.

About the Presenter: Sudhakar Reddy obtained his undergraduate degree in Electrical and Communication Engineeing from Osmania Unversity, M.S. degree from Indian Institute of Science, and Ph.D. degree in Electrical Engineering from the University of Iowa, Iowa City, Iowa. Dr. Reddy has been active in the areas of testable designs and test generation for logic circuits since 1972. He has been an associate editor and twice a guest editor of IEEE Transactions on Computers. He was Program Committee Chair for 1989 International Symposium on Fault- tolerant Computing. Since 1968 he has been a member of the faculty of the Department of Electrical and Computer Engineering, University of Iowa, where he is currently the Department Chairman. In 1990 he was made a University of Iowa Foundation Distinguished Professor. In 1995 he received the Von Humboldt Senior Researcher Fellowship. He is currently an associate editor of IEEE Transcations on CAD. He is a Fellow of IEEE.

Dr. Reddy has served on the Technical Advisory Board of Sunrise Test Systems. He has been a consultant to Honeywell Inc, AT&T Bell Labs, Rockwell-Collins, and Mentor Graphics. Dr. Reddy has presented tutorials on Delay Fault Testing at International Test Conference for several years.

Tutorial 2: *SoC Testing & P1500 Standard*

Monday, Dec. 4, 8:30 am-12:00 pm and 1:30 pm-5:00 pm; R105

Presenter: Y. Zorian , LogicVision, USA

Chair: Tsin-Yuan Chang, National Tsing Hua University, Taiwan

Audience: Designers, test engineers and researchers interested in learning about the state-of-the-art in embedded test methods for complex systems-on-chip and beyond.

Description: Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. This tutorial presents the state-of-the-art in system-level integration and addresses the strategies and current industrial practices in the test of system-on-chip. It discusses the requirements for test reuse in hierarchical design, such as embedded test strategies for individual cores, test access mechanisms, test interface standardization, optimizing test resource partitioning, and embedded test management and integration at the System-on-Chip level.

About the presenter: Yervant Zorian is the Chief Technology Advisor of LogicVision Inc. Previously, he was a Distinguished Member of Technical Staff at Bell Labs, Lucent Technologies, Test and Reliability Center of Excellence. His activities include the areas of embedded core, IC and Multi-Chip Module DFT methodologies. Zorian received an MSc degree from the University of Southern California, and a PhD from McGill University. He is currently the Editor-in-Chief of IEEE Design & Test of Computers. He founded and chairs the TECS workshop; and the IEEE P1500 Embedded Core Test Standardization Working Group. He has provided tutorials and courses at numerous conferences and academic programs (such as ITC, ICCAD, DATE, VTS, ETW, etc). He was granted several patents in the domain of embedded test and received a number of Best Paper Awards. He is a Fellow of IEEE.

ATS Activity Meetings

- **Asian Test Committee Meeting**
  Monday, Dec. 4, 4:00 pm-5:30 pm; R101

- **ATS Tenth Anniversary Committee Meeting**
  Tuesday, Dec. 5, 12:00 pm-13:00 pm; R101

- **ATS Tenth Anniversary Compendium Editorial Committee**
  Dec. 5-6, 8:30 am-6:00 pm; R101

Plenary Sessions

Opening Remarks

Tuesday, Dec. 5, 8:10 am - 8:30 am; R100

Cheng-Wen Wu, General Chair

Kuen-Jong Lee, Program Co-chair

Chau-Chin Su, Program Co-chair

Presentation of IEEE Computer Society Service Awards

By Kozo Kinoshita, Asian Group Chair, Test Technology Technical Council

To:

Dr. Vishwani D. Agrawal, AT&T Bell Laboratories, USA

Dr. Ben M. Y. Hsiao, IBM, USA

Prof. Yashwant K. Malaiya, Colorado State University, USA

Prof. Shiyi Xu, Shanghai University, China

Keynote Speech I: *Testing in the Fourth Dimension*

Tuesday, Dec. 5, 8:30 am – 9:20 am; R100

Speaker: Vishwani D. Agrawal, Bell Labs.

Chair: Kwang-Ting (Tim) Cheng, UCSB, USA

Abstract: Digital testing in the last three decades has taught us the value of design for testability (DFT). Disciplines such as scan and built-in self-test (BIST) have emerged as standard practices because they allow logic testing of arbitrarily large systems. This has been one of the greatest achievements in testing thus far. These past decades have also produced significant advances in semiconductor technology, which make extremely fine features and larger scales of integration possible. The beginning of the new millennium is an era of

the system-on-a-chip (SoC). Today's specialized SoCs will soon become large-volume production chips and there will lie our testing challenge of the new millennium.

Those SoCs will contain mixed signal subsystems. Testing of analog parts has always required accurate generation and analysis of timing waveforms. Digital subsystems of the future SoCs can be characterized as ultra-high speed devices whose clock-rates will exceed any affordable automatic test equipment (ATE). Besides, the signal integrity of ATE to device under test interface will be a major source of yield loss. If we can learn from the experience of the past, DFT, though not necessarily the same DFT, should be the answer. I do not mean that a BIST-based speed test will have the ATE go away. I think the future design styles will explore new DFT methods for timing test that are similar to scan only in spirit. For example, high-speed clocks and other time-critical waveforms may be generated on chip by locally embedded circuitry (modified flip-flops, DSP, filters, etc.) So, the challenge for the future is to find a timing analog of “scan” that will allow both logic and timing tests of arbitrarily complex systems and also permit simple tests to ascertain the integrity of the DFT hardware.

About the Speaker: Vishwani D. Agrawal is a Distinguished Member of Technical Staff at Bell Labs, Murray Hill, New Jersey, USA, and a Visiting Professor at Rutgers University, New Brunswick, New Jersey, USA. He received a BSc degree from Allahabad University, Allahabad, India, in 1960, BE degree from University of Roorkee, Roorkee, India, in 1964, ME degree from the Indian Institute of Science, Bangalore, India, in 1966, and a PhD degree from the University of Illinois at Urbana-Champaign in 1971. In 1986, he was elected an IEEE Fellow for his contributions to “probabilistic testing of integrated circuits.” In 1993, University of Illinois honored him with their Distinguished Alumnus Award. In 1998, he received the Harry H. Goode Award of the IEEE Computer Society for “innovative contributions to the field of electronic testing.” He has published 250 papers and five books, and has received five best paper awards. He holds twelve U.S. patents on testing and low-power design. He has co-directed 12 PhD theses at major universities. In 1991 he co-founded the International Conference on VLSI Design. He is a former editor-in-chief (1985-87) of the IEEE Design & Test of Computers and the founding editor-in-chief (since 1990) of the Journal of Electronic Testing: Theory and Applications. He was the program chair for the Fourth IEEE Asian Test Symposium. He serves on the ECE Alumni Board of the University of Illinois and the ECE Advisory Board of the New Jersey Institute of Technology.

Keynote Speech II: *Challenges for the Academic Test Community*

Tuesday, Dec. 5, 9:20 am – 10:10 am; R100

Speaker: Melvin A. Breuer, U. of Southern California

Chair: Kwang-Ting (Tim) Cheng, UCSB, USA

Abstract: These are exciting times for digital technology, as we see continual reductions in feature size and power supply voltage, and increases in chip size, density and speed. Unfortunately, test costs seem to demand an increasing fraction of the total production costs. Are we failing industry?

Over the last 20 years many active areas of research have emerged, such as ATPG, fault simulation, diagnosis, scan design, boundary scan, IDDQ testing, delay and at-speed testing. In this talk I will focus on the academic contributions in some of these areas. I will address the question of whether researchers are targeting yesterdays problems, problems that industry will address in 1-2 years, or problems they will address in 5-10 years. Is most of our work incremental? Are we doing evolutionary or revolutionary research? As and example, we see a continual stream of papers on improving ATPG efficiency and test compaction? Are these the key problems in test pattern generation that need to be addressed? What about multiple clock domains, tri-state logic, bi-directional logic, dynamic logic, transistor primitives and latch-based designs?

At one end of the design spectrum designers have been using VERILOG and VHDL to describe their designs. Now signal processing engineers want to define their designs in C. How can we make these synthesized designs testable? Better yet, who is addressing the problem? At the other end of the spectrum, engineers are addressing low level issues such as noise (e.g. crosstalk), process variation and ground bounce. Is academia adequately looking at these problems?

Finally I will touch on the relationship between industry and academic research from the perspective of funding, sharing of data and distribution of software.

About the Speaker: Melvin A. Breuer received his Ph.D. in electrical engineering from the University of California, Berkeley, is currently a Professor of both Electrical Engineering and Computer Science at the University of Southern California, Los Angeles, California, and is the Charles Lee Powell Professor of Computer Engineering. He was Chairman of the Department of Electrical Engineering-Systems from 1991-1994. His main interests are in the area of computer aided design of digital systems, design-for-test and built-in self-test, and VLSI circuits.

Dr. Breuer is the editor and co-author of Design Automation of Digital Systems: Theory and Techniques, Prentice-Hall; editor of Digital Systems

Design Automation: Languages, Simulation and Data Base, Computer Science Press; co-author of Diagnosis and Reliable Design of Digital Systems, Computer Science Press; co-editor of Computer Hardware Description Languages and their Applications, North-Holland; co-editor and contributor to Knowledge Based Systems for Test and Diagnosis, North-Holland; and co-author of Digital System Testing and Testable Design, Computer Science Press 1990 and reprinted in 1995 by the IEEE Press. He has published over 200 technical papers and was formerly the editor-in-chief of the Journal of Design Automation and Fault Tolerant Computing, on the editorial board of the Journal of Electronic Testing, the co-editor of the Journal of Digital Systems, and the Program Chairman of the Fifth International IFIP Conference on Computer Hardware Description Languages and Their Applications. He was co-author of a paper that received an honorable mention award at the 1997 International Test Conference. He is a Fellow of the IEEE; was a Fullbright-Hays scholar (1972); received the 1991 Associates Award for Creativity in Research and Scholarship from the University of Southern California, the 1991 USC School of Engineering Award for Exceptional Service, and the IEEE Computer Society's 1993 Taylor L. Booth Education Award. He was Chair of the Faculty of the School of Engineering, USC, for the 1997-98 academic year.

Industry Sessions

Industry Session I: *CAD Tools on Testing*

Tuesday, Dec. 5, 10:30 am – 12:00 pm; R100
Session Chair: Jing-Yang Jou, NCTU, Taiwan

10:30-10:45 DFT and BIST Techniques for the Future
Hsin-Po Wang, SynTest Technologies, Inc., Taiwan and
Jon Turino, SynTest Technologies, Inc., USA
10:45-11:00 DFT Closure
F. Hayat, T.W. Williams, R. Kapur and D. Hsu, Synnpsys Inc., USA
11:00-11:15 Current Status and Future Trend on CAD Tools for VLSI Testing
Wu-Tung Cheng, Mentor Graphics Corporation, USA
11:15-11:30 Yervant Zorian
11:30-12:00 Discussion

Industry Session II: *Taiwan Test Industry: Value Added Testing in the New Millennium*

Tuesday, Dec. 5, 1:30 pm – 3:00 pm; R100
Session Chair: Chung-Len Lee, NCTU, Taiwan
Participants: Chih-Yuan Lu, Ardentec Ltd., Taiwan
Charles Yeh, Chroma Ltd., Taiwan
Michael Chao, Davicom Ltd., Taiwan
L.T. Wang, Syntest Ltd.
Ching-Tin Lin, TSMC, Taiwan

Abstract: In the last two decade of the 20th century, the integrated circuit (IC) industry has prolonged and redefined Taiwan Economic Miracle. The rally has passed from OEM to IDM then to the foundry services. With the strong supports from the foundry and manufacturing sectors, the energetic and creative design sector has seen a unsurpassed opportunity in the new Millennium. The shift in the paradigm will have a significant impact on the test sector. In Taiwan Test Industry Session, we will discuss how the test sector shall react, what the emerging technologies are, and what the new business protocol should be from designer, test house, and ATE suppliers respectively.

Fringe meeting

Topic: SoC *Testing & P1500 Standard*

Wednesday, Dec. 6, 8:00 am – 9:35 am; R105
Chair: Shianling Wu, Lucent, USA
Co-chair: Yervant Zorian, LogicVision, USA

Participants:		
	Xinghao Chen	IBM, USA
	Martin Fischer	Agilent, Germany
	Douglas Kay	Cisco, USA
	J.C. Frank Lien	Actel, USA
	Phil Smith	Teradyne, USA
	L.T. Wang	SynTest, Taiwan

Panel Discussions

Panel 1: *Mixed-Signal Testing: Is Mixed-Signal Design-for-Test on Its Way?*

Tuesday, Dec. 5, 3:15 pm – 4:45 pm; R110

Moderator: Chin-Long Wey, Michigan State University, USA

Panelists:

Adam Osseiran, Fluence Technology Inc. (Europe), Switzerland
Jose Luis Huertas, Instituo Microelectronica de Sevilla-CNM, SPAIN
Yeon-Chen Nieu, Teradyne, Taiwan

Abstract: The world market for electronic systems will reach $1 Trillion within a year and with further exponential growth over the next five years. The growth in areas such as telecommunications has increased the demand for creating single chip solutions to system. This has been achieved by integrating a number of complex sub-systems, including standard interface blocks (e.g., analog/ digital converters), reused design cores (e.g., memory or microprocessors), embedded software, and new, innovative, custom designed "user blocks", into a single chip. Today, system-on-a-chip (SoC) has become a reality. However, the complexity of SoC makes it very difficult to achieve the desire test coverage without affecting the design schedule.

In the last decade, testing complex digital ICs has dramatically improved. Fully automated test solutions are commercially available. DFT (design-for-test) and BIST (Built-in-self-test) methodologies have been well-developed and available for today's high-complexity and/or high performance designs. However, mixed-signal DFT is far behind. This is simply due to the lack of standard fault model for analog circuits, standard mixed-signal DFT methodology, and commercially available ATPG for mixed-signal circuits. A number of DFT and BIST design methods of analog modules, such as ADC, DAC, PLL, analog front end circuits, and etc., have been developed by university researchers. Due to high testing cost, many companies are still not willing to make efforts to perform testing on analog modules like embedded PLLs.

In order to improve SoC design productivity, efficient SoC test methods must be developed and commercially available. This panel will address the following interesting issues:

- Is toady's mixed-signal DFT methodology on its way to resolve the challenges of today's industrial market demanding?
- Is BIST the mixed-signal DFT solution?
- Is embedded test the mixed-signal test solution?

Panel 2: *Collaboration between Industry and Academia in Test Research*

Tuesday, Dec. 5, 3:15 pm – 4:45 pm; R105

Moderator: Kwang-Ting (Tim) Cheng, UCSB, USA

Panelists:

Vishwani Agrawal, Bell Labs, USA
Jing-Yang Jou, NCTU, Taiwan
Li-C. Wang, Motorola/UCSB, USA
Chi-Feng Wu, Philips, Taiwan
Shianling Wu, Lucent, USA

Abstract: Even though there is a great need for innovative advances and excellent research opportunities in test and diagnosis, various issues faced by academic and industrial test researchers seem to make it harder to perform research that could create wide impact to the industry. Diversifying technologies, limited access to design and manufacturing data, increasing cost for building required infrastructure for experiments with reasonable scale, application-specific nature of test solutions, etc. are among those often cited issues.

The panel will discuss how academia and industry have contributed to test technology in the past, evaluate the current health of academic and industrial test research and explore how academia and industry can collaborate to meet the challenges in test and to increase its impact to the industry.

Specifically, the panel will discuss the following topics: What collaboration models between university and industry in the test area are most/least successful? What are the emerging research topics that academic or industrial research is ill-equipped to make real contributions? Will promoting the academic test research to "get real", "get practical", and "work closely with industry", adversely discourage high risk, "long term" basic research and pursuing major breakthroughs?

Technical Paper Sessions

Session A1: *Analog & Mixed Signal Test I*

Tuesday, Dec. 5, 4:45 pm – 6:00 pm; R110

Chair: *Kiyoshi Furuya, Chuo University, Japan*

A1-1 Test Generation for Fault Isolation in Analog Circuits Using Behavioral Models
S. Cherubal and A. Chatterjee

A1-2 Fault Diagnosis for Linear Analog Circuits
J.-W. Lin, C.-L. Lee, C.-C . Su, and J.-E. Chen

A1-3 Testing Mixed-Signal Cores: Practical Oscillation-Based Test in an Analog Macrocell
G. Huertas, D. Vazquez, E. Peralías, A. Rueda, and J. Huertas

A1-4 New Built-In Self-Test Technique Based on Addition/Subtraction of Selected Node Voltages
K. Ko and M. Wong

Session A2: *Memory Built-In Self-Test and Self-Diagnosis*

Tuesday, Dec. 5, 4:45 pm – 6:00 pm; R105

Chair: *Ad J. van de Goor, Delft University of Technology, Netherlands*

A2-1 A Built-In Self-Test and Self-Diagnosis Scheme for Embedded SRAM
C.-W. Wang, C.-F. Wu, J.-F. Li, C.-W. Wu, T. Teng, K. Chiu, and H.-P. Lin

A2-2 An FPGA-Based Re-Configurable Functional Tester for Memory Chips
J.-R. Huang, C. Ong, K. Cheng, and C. Wu

A2-3 BIST TPG for SRAM Cluster Interconnect Testing at Board Level
C.-H. Chiang and S. Gupta

A2-4 Efficient Built-In Self-Test Algorithm for Memory
S.-J. Wang and C.-J. Wei

Session B1: *Analog & Mixed Signal Test II*

Wednesday, Dec. 6, 8:00 am – 9:35 am; R110

Chair: *M.D. Shieh, National Yunlin Technical University, Taiwan*

B1-1 Optimal Test-Set Generation for Parametric Fault Detection in Switched Capacitor Filters
W. Choi, R. Harjani, and B. Vinnakota

B1-2 TI-BIST: A Temperature Independent Analog BIST for Switched-Capacitor Filters
L. Carro, E. Cota, M. Lubaszewski, Y. Bertrand, F. Azaïs, and M.

Renovell

B1-3 Analog Circuit Equivalent Faults in the D.C. Domain
M. Worsman, M. Wong, and Y. Lee

B1-4 A Methodology for Fault Model Development for Hierarchical Linear Systems
Y.-C. Huang, C.-L. Lee, J.-W. Lin, J.-E. Chen, and C.-C. Su

B1-5 Testing a PWM Circuit Using Functional Fault Models and Compact Test Vectors for Operational Amplifiers
J. Calvano, V. Alves, and M. Lubaszewski

Session B2: *Fault Simulation & Timing Simulation*

Wednesday, Dec. 6, 8:00 am – 9:35 am; R102

Chair: *Kazumi Hatayama, Hitachi, Japan*

B2-1 A New Framework for Static Timing Analysis, Incremental Timing Refinement, and Timing Simulation
L.-C. Chen, S. Gupta, and M. Breuer

B2-2 On the Feasibility of Fault Simulation Using Partial Circuit Descriptions
I. Pomeranz and S. Reddy

B2-3 Fsimac: A Fault Simulator for Asynchronous Sequential Circuits
S. Sur-Kolay, M. Roncken, K. Stevens, P. Chaudhuri, and R. Roy

B2-4 Simulation of Resistive Bridging Fault to Minimize the Presence of Intermediate Voltage and Oscillation in CMOS Circuits
A. Keshk, Y. Miura, and K. Kinoshita

B2-5 Non-Invasive Timing Analysis of IBM G6 Microprocessor L1 Cache Using Picosecond Imaging Circuit Analysis
S. Polonsky, M. Mc Manus, D. Knebel, S. Steen, and P. Sanda

Session C1: *Fault Analysis I*

Wednesday, Dec. 6, 9:55 am – 11:10 am; R110

Chair: *Shiyi Xu, Shanghai University of Science and Technology, China*

C1-1 An Experimental Analysis of Spot Defects in SRAMs: Realistic Fault Models and Tests
S. Hamdioui and Ad J. van de Goor

C1-2 Enhanced Untestable Path Analysis Using Edge Graphs
S. Kajihara, T. Shimono, I. Pomeranz, and S. Reddy

C1-3 A Waveform Simulator Based on Boolean Process
L. Li, X. Yu, C.-W. Wu, and Y. Min

C1-4 On the Superiority of DO-RE-ME / MPG-D over Stuck-at-Based Defective Part Level Prediction
J. Dworak, M. Grimaila, B. Cobb, T-C. Wang, Li-C. Wang, and M.

Mercer

Session C2: *Test Generation I*

Wednesday, Dec. 6, 9:55 am – 11:10 am; R102

Chair: *Yukihiro Iguchi, Meiji University, Japan*

C2-1 Compaction-Based Test Generation Using State and Fault Information
A. Giani, S. Sheng, M. Hsiao, and V. Agrawal

C2-2 Test Sequence Compaction for Sequential Circuits with Reset States
Y. Higami, Y. Takamatsu, and K. Kinoshita

C2-3 SPIRIT: Satisfiability Problem Implementation for Redundancy Identification and Test Generation
E. Gizdarski and H. Fujiwara

C2-4 Forecasting the Efficiency of Test Generation Algorithms for Digital Circuits
S. Xu and W. Cen

Session C3: *Functional Testing*

Wednesday, Dec. 6, 9:55 am – 11:10 am; R105

Chair: *Tomoo Inoue, Hiroshima City University, Japan*

C3-1 Fast Hierarchical Test Path Construction for DFT-Free Controller-Datapath Circuits
Y. Makris, J. Collins, and A. Orailoğ lu

C3-2 Faster Processing for Microprocessor Functional ATPG
J. Hirase and S. Yoshimura

C3-3 Verification of Deadlock Free Property of High Level Robot Control
H. Hiraishi

C3-4 Functional Testing of Microprocessors with Graded Fault Coverage
R. Kannah and C. Ravikumar

Session D1: *Built-In Self-Test I*

Wednesday, Dec. 6, 11:20 am – 12:20 pm; R110

Chair: *Jacob Savir, New Jersey Institute of Technology*

D1-1 Single-Control Testability of RTL Data Paths for BIST
T. Masuzawa, M. Izutsu, H. Wada, and H. Fujiwara

D1-2 A BIST Methodology for At-Speed Testing of Data Communications Transceivers
S. Lin, S. Mourad, and S. Krishnan

D1-3 High-Speed Generation of LFSR Signatures
M.-D. Shieh, H.-F. Lo, and M.-H. Sheu

Session D2: *Software Testing & Test Synthesis*

Wednesday, Dec. 6, 11:20 am – 12:20 pm; R102

Chair: *Wen-Ben Jone, National Chung Cheng University, Taiwan*

D2-1 Strong Self-Testability for Data Paths High-Level Synthesis
X. Li, T. Masuzawa, and H. Fujiwara

D2-2 Generating Test Items for Checking Illegal Behaviors in Software Testing
M. Hirayama, J. Okayasu, T. Yamamoto, O. Mizuno, and T. Kikuno

D2-3 Using Genetic Algorithms for Test Case Generation in Path Testing
J.-C. Lin and P.-L. Yeh

Session D3: *Embedded-Core Testing*

Wednesday, Dec. 6, 11:20 am – 12:20 pm; R105

Chair: *Douglas Kay, Cisco, USA*

D3-1 A Hierarchical Test Control Architecture for Core Based Design
K.-J. Lee and C.-I. Huang

D3-2 Embedded Core Testing Using Genetic Algorithms
R. Xu and M. Hsiao

D3-3 Functional Testing and Fault Analysis Based Fault Coverage Enhancement Techniques for Embedded Core Based Systems
A. Bagwe and R. Parekhji

Session E1: *Memory Testing*

Wednesday, Dec. 6, 1:30 pm – 3:05 pm; R110

Chair: *Shih-Chieh Chang, National Chung Cheng University, Taiwan*

E1-1 Detection of SRAM Cell Stability by Lowering Array Supply Voltage
D.-M. Kwai, H.-W. Chang, H.-J. Liao, C.-H. Chiao, and Y.-F. Chou

E1-2 A Realistic Fault Model for Flash Memories
Y.-L. Horng, J.-R. Huang, and T.-Y. Chang

E1-3 Impact of Memory Cell Array Bridges on the Faulty Behavior in Embedded DRAMs
Z. Al-Ars and Ad J. van de Goor

E1-4 Memory Test Time Reduction by Interconnecting Test Items
W.-J. Wu and C. Tang

E1-5 An Efficient Parallel Transparent Diagnostic BIST
D. Huang and W. Jone

Session E2: *Test Generation II*

Wednesday, Dec. 6, 1:30 pm – 3:05 pm; R102

Chair: *Christian Landrault, LIRMM, France*

E2-1 Test Generation for Crosstalk-Induced Faults: Framework and

Computational Results
W.-Y. Chen, S. Gupta, and M. Breuer

E2-2 Testing Programmable Interconnect Systems: An Algorithmic Approach
B. Liu, F. Lombardi, and W. Huang

E2-3 Reducing Test Application Time for Full Scan Circuits by the Addition of Transfer Sequences
I. Pomeranz and S. Reddy

E2-4 TOF: A Tool for Test Pattern Generation Optimization of an FPGA Application-Oriented Test
M. Renovell, J. Portal, P. Faure, J. Figueras, and Y. Zorian

E2-5 Formal Verification of Data-Path Circuits Based on Symbolic Simulation
Y. Morihiro and T. Yoneda

Session E3:*IDDQ Testing*
Wednesday, Dec. 6, 1:30 pm – 3:05 pm; R105
Chair: *Sying-Jyan Wang, National Chung Hsing University, Taiwan*

E3-1 Is IDDQ Testing not Applicable for Deep Submicron VLSI in Year 2011?
C.-W. Lu, C.-L. Lee, C. Su, and J.-E. Chen

E3-2 High Speed IDDQ Test and Its Testability for Process Variation
M. Hashizume, H. Yotsuyanagi, M. Ichimiya, T. Tamesada, and M. Takeda

E3-3 Memory Reduction of IDDQ Test Compaction for Internal and External Bridging Faults
T. Maeda and K. Kinoshita

E3-4 A High-Speed IDDQ Sensor Implementation
Y. Antonioli, T. Inufushi, S. Nishikawa, and K. Kinoshita

E3-5 Cyclic Greedy Generation Method for Limited Number of IDDQ Tests
T. Shinogi, M. Ushio, and T. Hayashi

Session F1: *Built-In Self-Test II*
Wednesday, Dec. 6, 3:25 pm – 4:40 pm; R110
Chair: *Shianling Wu, Lucent, USA*

F1-1 Accelerated Test Pattern Generators for Mixed-Mode BIST Environments
W.-L. Wang and K.-J. Lee

F1-2 Effective Parallel Processing Techniques for the Generation of Test Data for a Logic Built-In Self Test System
P. Chang, B. Keller, and S. Paliwal

F1-3 Design and Testing of Fast and Cost Effective Serial Seeding TPGs Based on One-Dimensional Linear Hybrid Cellular Automata
A. Hlawiczka and M. Kopec

F1-4 An Efficient BIST Design Using LFSR-ROM Architecture.
L. Li and Y. Min

Session F2: *Testability Analysis and Design for Testability*
Wednesday, Dec. 6, 3:25 pm – 4:25 pm; R102
Chair: *Xinghao Chen, IBM, USA*

F2-1 Novel Techniques for Improving Testability Analysis
Y.-H. Su, C.-H. Cheng, and S.-C. Chang

F2-2 A Class of Sequential Circuits with Combinational Test Generation Complexity under Single-Fault Assumption
M. Inoue, E. Gizdarski, and H. Fujiwara

F2-3 Design for Sequential Testability: An Internal State Reseeding Approach for 100% Fault Coverage
M. Flottes, C. Landrault, and A. Petitqueux

Session F3: *Fault Tolerance*
Wednesday, Dec. 6, 3:25 pm – 4:40 pm; R105
Chair: *J.C. Frank Lien, Actel, USA*

F3-1 Testing Approach within FPGA-Based Fault Tolerant Systems
A. Doumar and H. Ito

F3-2 Transient-Fault Tolerant VHDL Descriptions: A Case-Study for Area Overhead Analysis
F. Vargas and A. Amory

F3-3 Fault Tolerant Multistage Interconnection Networks with Widely Dispersed Paths
N. Kamiura, T. Kodera, and N. Matsui

F3-4 A Testable/Fault-Tolerant FFT Processor Design
S.-K. Lu, J.-S. Shih, and C.-W. Wu

Session G1: *Fault Analysis II*
Wednesday, Dec. 6, 4:50 pm – 5:50 pm; R110
Chair: *Mike Wong, Hong Kong Polytechnic University, Hong Kong*

G1-1 Charge Sharing Fault Analysis and Testing for CMOS Domino Logic Circuits
C.-H. Cheng, W.-B. Jone, J.-S. Wang, and S.-C. Chang

G1-2 Testing Domino Circuits in SOI Technology
E. MacDonald and N. Touba

G1-3 A Case Study of Failure Analysis and Guardband Determination for a

64M-Bit DRAM
C.-T. Kao, S. Wu, and J. Chen

Session G2: *Low-Power Testing*
Wednesday, Dec. 6, 4:50 pm – 5:50 pm; R102
Chair: *C.P. Ravikumar, Indian Institute of Technology, India*

G2-1 Peak-Power Reduction for Multiple-Scan Circuits during Test Application
K.-J. Lee, T.-C. Huang, and J.-J. Chen

G2-2 An Adjacency-Based Test Pattern Generator for Low Power BIST Design
P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch

G2-3 Distribution-Graph Based Approach and Tree Growing Technique in Power-Constrained Block-Test Scheduling
V. Muresan, X. Wang, V. Muresan, and M. Vladutiu

Session G3: *Self-Checking Circuits and Concurrent Fault Detection*
Wednesday, Dec. 6, 4:50 pm – 5:45 pm; R105
Chair: *Yinghua Min, Academia Sinica, China*

G3-1 A Method for Determining Whether Asynchronous Circuits Are Self-Checking
M. Liebelt and C.-C. Lim

G3-2 On Testing Safety-Sensitive Digital Systems
J. Savir

G3-3 Accumulation-Based Concurrent Fault Detection for Linear Digital State Variable Systems
I. Bayraktaroglu and A. Orailoglu

Social Program

The 9th ATS is proudly to invite I Wan Jan Hand Puppet Theater to perform for us. Hand (glove) Puppetry, also called "Chang-Chung Hsi" (play in the palm), was introduced to Taiwan in the years of emperors Tao-kuang and Hsien-feng in the Ching dynasty and soon won local people's favor. In the early years, puppet shows were so widespread that their popularity could be compared with that of Taiwanese Opera. Owing to the relatively small size of troupes and productions that were less expensive than other types of drama, it became very popular and was performed in annual festivals and god-receiving pageants. Thus this humorous form of folk performance could be seen all across Taiwan, both day and night.

The I Wan Jan Hand Puppet Theater is one of the most prestigious hand puppetry troupes in Taiwan. I Wan Jan was founded by Lee Tien-Lu in 1931. Although he retired in 1978, I Wan Jan still performs in Taiwan and abroad as a non-profit performance group. Through the years, I Wan Jan has been invited to perform in various countries worldwide to introduce the art of hand puppetry, and to promulgate the beauty of this age-old art form. It has performed in Hong Kong, Korea, Japan, the United States, Italy, France, Luxembourg, Holland, Germany, Belgium, Canada, England, Portugal, Morocco, Austria, and Mainland China, among others. In addition to performance, I Wan Jan also places a lot of importance on education and development, striving to continue the tradition of hand puppetry. Lee's apprentices have established various related troupes all over the world. Students of the I Wan Jan troupe system are spread far and wide around the world, assuring the continuation of the delicate art of Chang Chung Hsi.
For more information on Hand Puppetry, please check the web page
http://www.cyberstage.com.tw/story/folkarts_e/poppet/p1.htm.
For more information on I Wan Jan Hand Puppet Theater, please check
http://www.cyberstage.com.tw/english/framef05.htm.

Tour Information

The Taiwan and Taipei tours can be arranged through Edison Travel Service. For detailed information and reservation, please check

http://www.edison.com.tw/eindex.htm.

Author/Presenter Index

Notations: A-G: Technical Sessions; K: Keynotes; FM: Fringe Meeting; P: Panels; T: Tutorials; AW: Awards; -0 is the chair.

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